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COPPER THERMOCOMPRESSION FOR MEMS ENCAPSULATION

Master's Programme in Chemical, Biochemical and Materials Engineering
Major in Chemistry

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Abstract of the master's thesis

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Abstract

Copper thermocompression is a promising wafer-level packaging technique, as it allows the bonding of electric contacts simultaneously to hermetic encapsulation. In thermocompression bonding the bond is formed by diffusion of atoms from one bond interface to another. The diffusion is inhibited by barrier forming surface oxide, high surface roughness and low temperature.

Aim of this study was to establish a wafer-level packaging process for MEMS (Micro-ElectroMechanical System) mirror and MEMS gyroscope. The cap wafer of the MEMS mirror has an antireflective coating that limits the thermal budget of the bonding process to 250°C. This temperature is below the eutectic temperature of most common eutectic bonding materials, such as Au-Sn (278°C), Au-Ge (361°C) and Au-Si (370°C). Thus a thermocompression bonding method needed to be developed. Copper was used as a bonding material due to its low cost, high self-diffusivity and resistance to oxidation in ambient air. The bond structures were fabricated using three different methods and the bonding was further enhanced by annealing. The bonded structures were characterized with scanning acoustic microscopy, scanning electron microscope and the bond strength was determined by shear testing.

Exposing the bond structures to etchant during Cu seed layer removal was found to drastically increase the surface roughness of bond structures. This increase proved detrimental to bond strength and dicing yield and thus covering the bond surface during wet etching is recommended. The native oxidation on copper surfaces was completely removed with combination of *ex situ* acetic acid wet etch and *in situ* forming gas anneal. Successful thermocompression bonding process using sputtered copper films was established at a low temperature of 200°C, well below the thermal limitation set by the antireflective coating. The established wafer bonding process had high yield of 97% after dicing. The bond strength was evaluated by maximum shear strength and recorded at 75 MPa, which is well above the MIL-STD-883E standard (METHOD 2019.5) rejection limit of 6.08 MPa.

Keywords Wafer-level packaging, thermocompression bonding, wafer bonding, MEMS, Cu

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Tiivistelmä

Kuparin lämpöpuristusliitäntä on lupaava kiekkotason pakkausmenetelmä, sillä se mahdollistaa sekä sähköisten liitäntöjen, että hermeettisen suljennan toteuttamisen samanaikaisesti. Lämpöpuristusliitännässä sidos muodostuu atomien diffuusiosta liitospinnalta toiselle. Diffuusiota rajoittavat estokerroksen muodostava pinta oksidi, korkea pinnan karheus ja matala lämpötila.

Diplomityön tavoitteena oli luoda kiekkotason pakkausmenetelmä mikroelektromekaaniselle (MEMS, MicroElectroMechanical System) peilille ja MEMS gyroskoopille. Peilin lasisen kansikiekon pinnalla oleva antiheijastava kalvo rajoitti liitännässä käytettävän lämpötilan korkeintaan 250°C:een, mikä on alempi lämpötila kuin useimpien kiekkoliitännässä käytettyjen materiaaliparien eutektinen piste. Esimerkkinä mainittakoon mm. Au-Sn (278°C), Au-Ge (361°C) ja Au-Si (370°C). Kuparin alhainen hinta, korkea ominaisdiffuusio ja hidas hapettuminen ilmakehässä puoltavat sen valintaa liitäntämateriaaliksi. Liitäntärakenteet valmistettiin kolmella menetelmällä ja liitännän vahvuutta parannettiin lämpökäsittelyllä. Liitetyt rakenteet karakterisoitiin pyyhkäisy elektronimikroskoopin, akustisen mikroskoopin ja liitoslujuus-mittauksen avulla.

Liitospintojen altistamisen hapolle havaittiin lisäävän pinnankarkeutta ja olevan siten haitallista liitokselle ja laskevan saantoa. Liitospintojen suojaaminen siemenkerroksen syövytyksen aikana on suotavaa. Pintaoksidi pystytään poistamaan täysin suorittamalla oksidin märkäetsaus jääetikalla sekä lämpökäsittely N_2/H_2 atmosfäärissä. Sputteroidut kuparikalvot pystyttiin liittämään onnistuneesti yhteen 200°C lämpötilassa, mikä on alle anti-heijastavan pinnan asettaman lämpötilarajan. Tällä liitäntä menetelmällä saavutettiin kiekkoliitoksella yhteen liitettyjen sirujen sahauksessa korkea 97% saanto. Liitoslujuus määritettiin maksimi-leikkausvoiman avulla ja sen suuruudeksi mitattiin 75 MPa. Lujuus oli yli kymmenkertainen MIL-STD-883E standardin (METHOD 2019.5) asettamaan hylkäysrajaan 6.08 MPa nähden.

Avainsanat Kiekkojen pakkaus, lämpöpuristusliitäntä, piikiekkoliitäntä, MEMS, Cu

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5.4.2019 Espoo, Finland

Henri Ailas

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List of abbreviations

AR = Anti-reflective. Antireflective coatings are typically made of several metal oxide layers, such as SiO_2, TiO_2 and MgF.

BEOL = Back end of line. Part of IC fabrication, where individual devices are interconnected with wiring.

CMOS = Complementary metal-oxide-semiconductor. A transistor composed of n- and p-type semiconductors.

CMP = Chemical mechanical polishing. Process where surface is smoothened using abrasive and corrosive slurry on a polishing pad.

EDS = Electron dispersion spectrometry. Chemical microanalysis technique used together with SEM.

IC = Integrated circuit. Set of electronic circuits on a single, small, piece of substrate.

IR = Infrared. Electromagnetic radiation corresponding to wavelengths from 700 nm to 1 mm.

LIDAR = Light Detection and Ranging. Distance measuring method where target is illuminated and reflected light is measured.

PEB = Post-exposure bake. Heat treatment of photoresist after exposure to UV-radiation.

R_a = Surface roughness. Deviations perpendicular to the ideal surface. Arithmetic mean of multiple measurements.

R_q = Surface roughness. Deviations perpendicular to the ideal surface. Root-mean-square of multiple measurements.

RT = Room temperature. Temperature between 20°C and 25°C.

SAM = Scanning acoustic microscope. Microscope that uses sound to produce an image. Commonly used for failure analysis, such as detecting voids or cracks in microelectronic packages.

SAM = Self-assembled monolayer. Single molecule thick layer of organic molecules formed spontaneously on surface by adsorption.

SEM = Scanning electron microscope. Microscope that uses a focused electron beam to produce an image. Typically used to obtain information on sample topography and composition.

SOI = Silicon on insulator. A substrate composed of layered structure of silicon-insulator-silicon, it is used in place of normal silicon substrates to reduce parasitic device capacitance.

SSP = Single side polished. A Silicon wafer that has polished front side and matt backside.

TSV = Through-silicon via. Vertical electrical connection that passes through silicon wafer.

UV = Ultraviolet. Electromagnetic radiation with wavelengths from 10 nm to 400 nm.

WEC = Wedge error compensation. Step in lithography where the wafer and mask are parallelized.

XPS = X-ray photoelectron spectroscopy. Surface sensitive spectroscopic technique used in measuring the elemental composition of sample.

Materials

$FeCl_3$ = Iron(III) chloride, also known as ferric chloride

HCl = Hydrochloric acid

HMDS = Hexamethyldisilazane, also known as Bis(trimethylsilyl)amine

HNO_3 = Nitric acid

H_2O_2 = Hydrogen peroxide

H_3PO_4 = Phosphoric acid

$Na_2S_2O_8$ = Sodium persulfate, also known as Sodium peroxodisulfate

NH_3 = Ammonia

Symbols

α = Coefficient of thermal expansion

ΔH = Reaction enthalpy

G = Interfacial adhesion energy

ν = Poisson's ratio

E = Elastic modulus

P = Load, in four point bending test.

h = Distance between inner and outer loading points, in four point bending test

b = Sample width, in four point bending test.

h = Sample thickness, in four point bending test.

1 Introduction

The thesis was motivated by need to develop a wafer level packaging method for hermetic encapsulation. There are two main methods for wafer bonding: eutectic and thermocompression bonding. In eutectic bonding an eutectic solder is created from two metals which can be liquefied at a specific temperature. When cooled these form a single solid phase. In eutectic bonding controlling solder in liquid phase poses challenges, the flowing bond material can ruin the encapsulated device. The most common eutectic bond material is Au-Si.

Hence, increasing interest has been directed towards thermocompression bonding. In thermocompression bonding two materials are compressed to each other and diffusion of atoms between the bonding interface, facilitated by heat, bonds the interfaces together. The diffusion leads to original bond interface slowly disappearing as two solid phases morph into one.

The study of diffusion bonding has mainly focused around three metals: gold, copper and aluminum. Of these materials aluminum oxidizes easily in ambient atmosphere creating a thin layer of aluminum oxide on top of all aluminum surfaces. Hence, in bonding, there is an aluminum oxide layer between the two bonding interfaces, inhibiting diffusion of Al atoms from one interface to another. To overcome this hindrance a high temperature and compression force has to be used. Gold, however, does not readily oxidize in atmosphere and is in that sense an excellent material for thermocompression bonding. The largest disadvantage of gold is its high cost, being several orders of magnitude higher than that of aluminum and copper. Copper is in the same price range as aluminum and while it does oxidize in ambient atmosphere, the oxidation reaction is slow and occurs over a long period of time.

Because of coppers benefits over the Au and Al this thesis only studies copper thermocompression bonding. The study focused on bonding parameters such as temperature and pressure as well as surface cleaning and fabrication of bonded copper films.

The aim of the work was to establish a process for wafer level diffusion bonding of patterned copper structures at temperatures of 250°C or lower.

2 Wafer bonding for MEMS encapsulation

The chapter describes shortly two MEMS devices that are the target of the wafer level packaging process developed in the thesis. The three most common thermocompression bonding metals and their bonding parameters are presented, with focus on copper. For copper thermocompression bonding various pretreatment methods are introduced as well as the effect of surface conditioning and thermal treatment. Fabrication and characterization of copper structures as well as characterization of bonded wafers are discussed.

2.1 Micro-Electro-Mechanical Systems

An overview of microelectromechanical systems with focus on two MEMS devices, gyroscope and micro mirror. Their functionality are described, to understand the bonding limitations caused by the two target devices. In addition, the economical impact of MEMS technology is examined briefly.

2.1.1 Introduction to MEMS

The acronym MEMS comes from Micro-Electro-Mechanical Systems which can be defined as miniaturized mechanical and electromechanical elements, made using microfabrication [1]. The variety of MEMS devices ranges from simple elements with no moving parts to complex designs of multiple moving parts controlled by integrated microelectronics. Similarly, their size can vary from sub-micron to several millimeters. In this sense, MEMS and Nanotechnology, generally considered as separate categories, are both used to describe highly miniaturized devices. In a way, they are two different labels used to describe the same technology [2]. The functional elements of MEMS can be categorized as sensors, actuators, microelectronics and microstructures [2]. A closer look is taken into a MEMS gyroscope and a micro mirror, as they are the target of the capping process developed in the thesis.

Looking MEMS from economical point of view, the global MEMS market was valued at $13 billion in 2015 [3]. Moreover, according to Singh at Allied Market Research it is expected to grow to $26.8 billion by 2022 [3]. The largest individual factors credited for the growth are high adoption in smartphones, demand in automation industry and increasing popularity of the Internet of Things [3].

2.1.2 Gyroscope

Historically gyroscope is a devise with a spinning mass and due to Newton's 1st law the spinning object will persist to keep its orientation when the device is turned [4]. An exemplary MEMS gyroscope is depicted in Fig. 1, as can be seen the device consists both vibrating ring and tuning fork design. They are the two of the most common designs in MEMS gyroscopes [5].

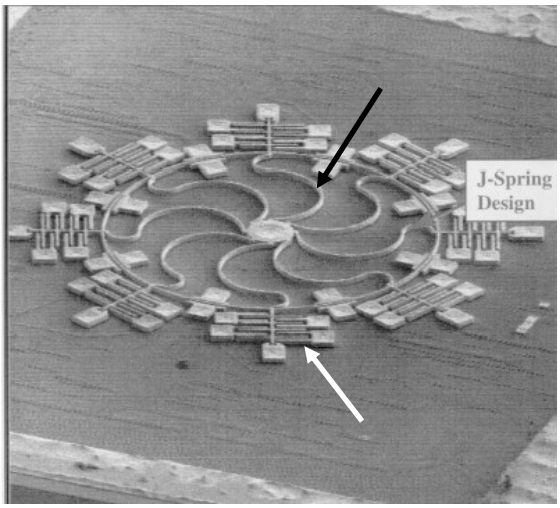

Fig. 1: Exemplary image of a MEMS gyroscope. Several tuning forks (white arrow) surround the large vibrating ring, indicated by black arrow. (Image from Douglas Sparks of Delco Automotive Systems) [5].

In a well working gyroscope the energy loss needs to be small. In a practical MEMS gyroscope the air dampening is the most significant factor. In short, energy loss occurs from collisions between MEMS resonators and gas particles. The energy loss is proportional to concentration and mean velocity of gas molecules, thus better performance is achieved in lower pressure [6].

Operating pressures of 300 Pa have been reported by Tsuchiya *et al.* [7], whereas some high-end pressure sensors and gyroscopes may need pressures lower than 10^{-2} Pa in the operating cavity [8]. Needless to say, the sealing of these components needs to be performed *in vacuo*. In packaging of gyroscopes the most important parameter for the seal ring is airtightness.

2.1.3 Micro mirror for LIDAR

Light Detection and Ranging, also known as LIDAR, is a distance measurement method. In LIDAR a pulse of light is emitted and its reflection form a surface is detected, the distance can be calculated from the time of flight using equation (1) [9].

$$\text{Distance} = \frac{\text{Speed of light} \times \text{Time of flight}}{2} \quad (1)$$

In a typical LIDAR, laser is used as a light source and a rotating mirror is used to direct the laser in a way that a surrounding area can be scanned. In current methods, this is done using relatively large macroscopic mirrors rotated by electric motors, which are prompt to mechanical wear and expensive [10]. Another drawback is their size and weight, which limits their possible application especially in the field of unmanned aerial vehicles [11].

There are several solutions for this problem. One is to use solid state application such as flash LIDAR or optical phased array antennas [10]. Alternatively, the mirror can be shrunk into microscale as seen in Fig. 2 [11] and made to operate without a separate motor. It is these microscopic MEMS mirrors, which VTT is developing. Packing of these MEMS devices has its own unique requirements. The light has to be able to

pass into the mirror, in other words the cap wafer has to be transparent in the wavelength of the used laser. Typically, some type of glass wafer is used for capping. The capping wafer can be augmented with optical coatings such as an anti-reflective coating to improve its optical transmittance. However, the coatings can cause restrictions to the bonding parameters and processing methods. The thermal stability of antireflective coating can limit the maximum process temperature to which the wafer can be exposed. The maximum operating temperature for the antireflective coating used in the thesis is 250°C, well below typical bonding temperatures.

Looking at previous research done on MEMS mirrors, Hofmann describes a use of glass fritz bonding in capsulation of MEMS mirror [12]. Glass fritz bonding typically requires temperatures around 430°C making it unusable in this application [13].

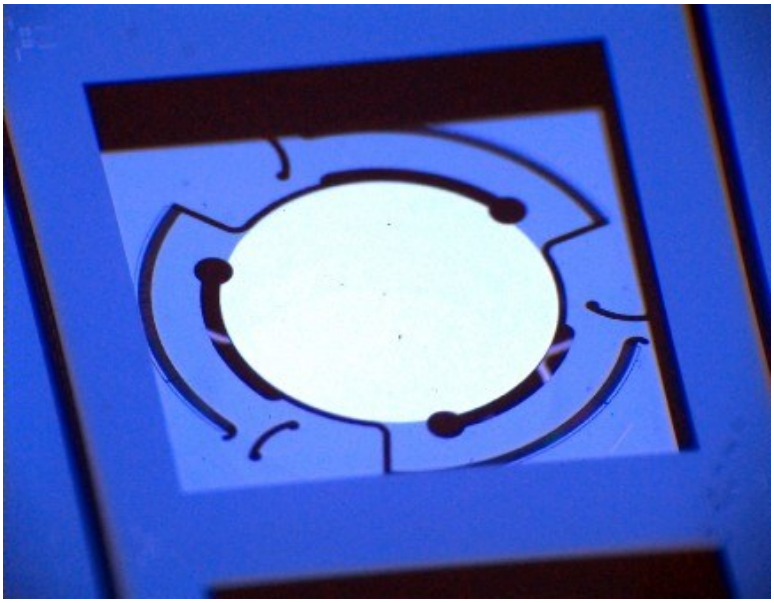

Fig. 2: MEMS mirror by Fraunhofer ISIT (Image from MiniFaros) [14].

2.1.4 Wafer level packaging of MEMS

In wafer level packaging, all of the chips in the wafer are bonded simultaneously as the device wafer is bonded to the cap wafer (Fig. 3). The method saves considerable

amount of time compared to chip bonding, where each chip is capped separately, especially if the chips are small. In short, bond frames are fabricated on both cap and device (MEMS) wafer, the wafers are pressed together and thus bond frames of all of the individual chips on the wafer are bonded simultaneously. After bonding, the back-side of the cap wafer can be grinded to reveal through silicon vias (TSV) which are used to conduct electricity inside the sealed cavity. Lastly, the wafer is diced into individual chips.

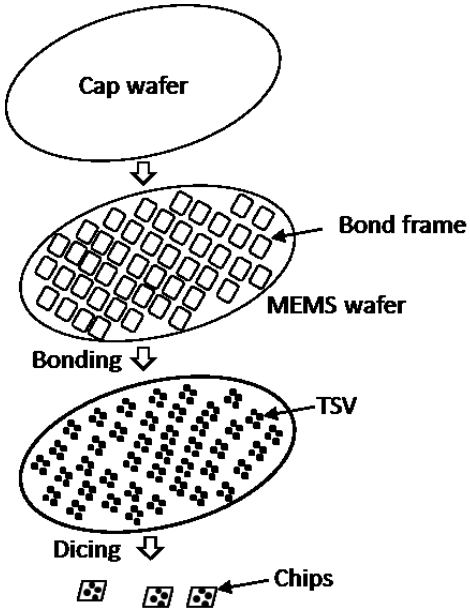

Fig. 3: Wafer level packaging process. Bonding the cap wafer to MEMS wafer encapsulates all of the chips simultaneously. After bonding, the cap wafer can be grinded to reveal TSV's and diced into individual chips.

2.2 Diffusion bonding materials and typical bonding parameters

Three of the most common diffusion bonding metals are presented and their benefits and drawbacks are discussed. As well as the typical thermocompression parameters, with focus on applied force and temperature. Comparison of the thermocompression related properties of the three metals Au, Al and Cu are summarized in Table 1.

2.2.1 Introduction to thermocompression bonding

Thermocompression bonding, also known as diffusion bonding, relies on solid-state diffusion of metal atoms between the two bond interfaces. The metals are pressed together at elevated temperatures and pressures to ease the diffusion between the interfaces [15]. Elevated pressure is used to minimize the distance between the bond interfaces caused by metals surface conditions. Elevated temperature is used to help the diffusion by increasing the kinetic energy of atoms [16].

Compared to other bonding methods, thermocompression bonding has several advantages. Typically, homogenous metals are used as bonding material. This simplifies the bond structure fabrication compared to eutectic bonding, where precisely controlled alloys are needed [15]. Another benefit is the lack of liquid phase in the bonding, there is no risk of liquid bond material overflowing and contaminating the device. A further drawback of eutectic bonding are low reflow temperatures, the melting point of formed alloy is often low and exposure of the bond to temperatures above it will re-melt the bond. For a commonly used eutectic alloy, gold tin alloy, the melting point is 278°C at tin content of 29 atomic-% [17]. However, the lack of liquid phase can also be a disadvantage, as the bond interphase cannot adapt to each other, the importance of low surface roughness becomes increasingly significant [15], [18]. Further drawback of thermocompression is that same material is needed for both bond interfaces, which is to say on both cap and device wafers. This can be a problem if the bond material is not compatible with CMOS process, like copper or gold, as contamination of tooling should be avoided.

The bond formation is based on atom-atom bonds followed by grain growth caused by metal atom diffusion [19]. Hence, the bond material needs to have good self-diffusivity, to reduce the bonding time. In addition, low activation energy is preferred for easy forming of atom-atom bonds between the interfaces, resulting in lower bonding temperatures [15]. The selected properties of Al, Au and Cu are presented in Table 1.

Table 1: Properties of the three most common thermocompression metals.

	Bonding Temperature (°C)	Bonding force (kN) [18]	Self-Diffusivity ($m^2 s^{-1}$) [15]	Activation Energy (eV) [15]	Coefficient of thermal expansion (ppm $°C^{-1}$) [20]
Gold	>260 [15]	>40 kN	1.0×10^{-18} – 1.0×10^{-19} (at 400°C)	1.81 eV	14.2
Aluminum	400-450 [21]	>70 kN	4.2×10^{-19} (at 500°C)	1.49 eV	23.6
Copper	180-400 [22]	>30 kN	4.5×10^{-14} (at 500°C)	2.19 eV	16.5

2.2.2 Gold

The most defining feature of gold is its good resistance to oxidation. Unlike Al and Cu, gold doesn't oxidize in air, and therefore it is not affected by diffusion inhibiting oxide layer [23]. Gold bonding can be carried out in relatively low temperatures. For example, a seal ring suitable for MEMS packaging was successfully bonded at temperatures of 320°C and 350°C using bonding pressures of 2.5 MPa and 1.3 MPa respectively [23]. The bonding has been successfully carried out in temperatures as low as 300°C with pressure of 7 MPa [24]. On four-point bend test the interfacial energy was found to be between 22 to 67 J m^{-2} for these bonding parameters [24].

Experiments for gold thermocompression bonding have been done in even lower temperatures [25], [26]. Tsau *et al.* have experimented on thermocompression bonding of two sputtered gold films. The wafers were bonded at temperatures of 260°C and 300°C using pressures from 30 to 120 MPa [26]. In the study it is recommended that gold film should be deposited on diffusion barrier films such as silicon oxide, as silicon diffusion to gold has been found to be disadvantageous to bonding [26], [24]. Surface treatment is needed to remove organic contamination prior to bonding, Tsau

et al. have used UV-ozone exposure. For bonding parameters, temperature and pressure of 260°C and 120 MPa were recommended [26]. The pressure can be lowered with a trade-off in bond quality.

Ang *et al.* found the bond strength to be nearly linearly dependent on bonding temperature [25]. Thus, obtaining good bond quality at low temperatures will be challenging. An interesting finding by Tsau *et al.* is that the bond time showed little effect on the overall bond quality [26]. Even bond times as low as 2 minutes can be used. This is aspect is great news for commercial use in MEMS fabrication as it means faster throughput of chips. A seal ring linewidth of around 50 µm was recommended for sufficient reliability of hermeticity of the sealing [26].

2.2.3 Aluminum

In wafer bonding, requirements for high force and high temperature are distinctive features for aluminum bonding. In MEMS encapsulation a bonding force of 9-60 kN at temperatures of 400-450°C have been reported [27], [21]. Compared to Au and Cu, the reported values are relatively high. The main reason behind the aluminum's need for such a high temperature and pressure compared to copper or gold is that it readily oxidizes in atmosphere, forming a hard, diffusion inhibiting Al_2O_3 layer [21].

Insufficient diffusion leads to poor bond quality. At temperature of 400°C dicing yields of bellow 50% were reported for seal rings of line with 100 µm and 200 µm, when bonding force of 18 kN (34.28 MPa) was used. Whereas increasing the temperature to 450°C at same bonding force (18 kN) results to dicing yields around 80-90%, at temperature of 550°C the yield is full 100% [21]. These results point to a clear temperature dependency in Al-Al diffusion bonding. A correlation between applied bonding force and dicing yield has also been reported. At 400°C force of 18 kN and 60 kN, corresponding to pressures of 34.28 MPa and 114.3 MPa respectively, resulted in dicing yields of below 47% and above 77% respectively [21]. In other words, the need for higher bonding temperature can be substituted with use of higher bonding force. However, contradictory information was also recorded. In their study, Malik *et al.*

also recorded bonding force of 36 kN leading to lower dicing yield compared to 18 kN at 400°C, however they did not clearly explain such anomaly [21].

Another drawback is aluminum's relatively high coefficient of thermal expansion, reported at 23.6 ppm $°C^{-1}$ [20]. Compared to silicon α = 2.59 ppm $°C^{-1}$ at 25°C it is an order of magnitude higher, which can lead to more stress in encapsulation at elevated temperatures [28], [15]. As gold and copper have both lower coefficient of thermal expansion and bonding temperature the thermal stress related issues are most severe on aluminum. On the other hand, a major benefit is that Al is CMOS compatible material, unlike Cu and Au [29].

2.2.4 Copper

Copper has several properties that make it highly desirable material in thermocompression bonding. It has good electrical and thermal dissipation characteristics and smooth bonding surfaces can be made using existing chemical mechanical polishing (CMP) methods [30]. Physical properties of copper are favorable as well. The self-diffusivity of copper is four to five orders of magnitude greater than that of aluminum and gold (Table 1) [15]. This is noteworthy as the bonding is caused by the diffusion of atoms from one interface to another.

Another major benefit of copper is its low price. In London raw materials exchange copper goes around 6168.00 $/ton which is 7.08 €/kg (8.10.2018) [31]. In comparison gold is sold at 1185.20 $/troy-ounce converted to euros this gives 43736.99 €/kg (8.10.2018) [32]. In other words, copper benefits of being four orders of magnitude cheaper than gold.

Research on multilayer wafer stacking of copper bonding films has been studied and successful results using thermocompression bonding have been found. Four wafers with Si/SiO_2 layer and Ta/Cu bonding layer were managed to stack with strong enough bonding to withstand mechanical grinding of the backside of the wafer and etching of the grinded backside. The stacking was noted to have failed after the bonding and etch-back of fifth-layer. The failure was hypothesized to have been caused by

too large wafer bow, which had increased from 3.9 µm on the pair of wafers to 26.3 µm when bonding the fourth [33].

Typically Cu-Cu compression bond needs temperatures above 300°C and long bonding times, over 30 min, however there are various methods for achieving successful bonding in low temperatures [33], [34]. One such method is coating the bonding surface with silver nanoparticles. In their study, Liu *et al.* found silver nanoparticles on copper surface to form a continuous Cu-Ag-Cu interface, almost free of voids, when bonded at 180°C for 5 min and annealed at 200°C for 25 min [22]. Lower bonding temperatures can also be achieved using various pretreatment methods, which are discussed below in more detail. Even bonding at room temperature (RT) has been achieved, however such method did require further annealing at 200°C [19]. Due to low material costs and possibilities of low temperature bonding copper was found as the best candidate for encapsulation of the previously discussed MEMS devices.

2.3 Grain formation in the bond interface

As previously discussed, thermocompression bonding is facilitated by diffusion of atoms from one interface to another. These diffused atoms will form into grains, as the temperature and pressure environment during bonding differs from deposition conditions, the formed grains will have different crystal structure. Below the effect of thermal treatment on grain formation is discussed. In addition, the effect of surface roughness on bond formation and quality was studied.

2.3.1 Thermal treatment

Annealing is a commonly used method for improving the bond quality. It is performed by heating the wafers in inert N_2 atmosphere after bonding, once the wafers have cooled to room temperature. The reasoning behind the annealing is that at elevated temperatures the crystal growth between the bond interfaces, started in the bonding, continues. Chen *et al.* have measured, using XRD (x-ray diffraction), the intensity of (111)-peak to decrease in bonding, while the intensity of (220)-peak increased.

Thus during bonding and annealing a change in grain orientation from (111) to (220) has been observed [35]. The change proves the recrystallization, facilitated by diffused atoms. The recrystallization is presented in a TEM image below, Fig. 4a is an image of sputtered Cu film, (111) orientation observed. In Fig. 4b, the bond interface can be seen and the Cu films have several grain orientations. After annealing at 400°C (Fig. 4c), crystal growth across the interface is observed [34].

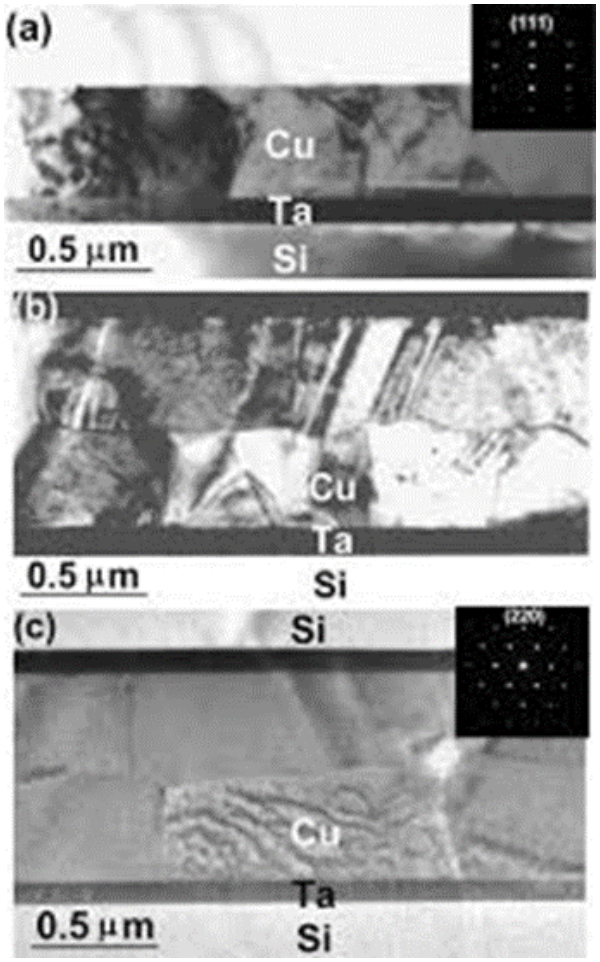

Fig. 4: TEM cross-section of Cu films. a) Sputtered Cu film, (111) orientation observed with XRD. b) Cu after bonding for 30 min. in 400°C. c) after bonding and 30 min anneal at 400°C, (220) grain orientation observed with XRD. Image from Chen et al. [34].

While the recrystallization is evident in the TEM images, the change grain orientation is better observed XRD diffraction patterns. In the top right corner of Fig. 4a the diffraction pattern is seen as blurry dots arranged in lines. Whereas, in the Fig. 4c the dots are more sharp and arranged in hexagonal pattern. The change in pattern indicates a change in grain orientation and the decrease in blurriness is result of bigger crystals. The difference between the two grain orientations is better visualized in Fig. 5.

The reason for the change in grain structure has been explained as energy and yield stress minimization [36]. The (220) grains have lower stress yields compared to (111) grains and their growth minimizes surface tension. In other word, the grain growth is precipitated by the stress minimization [16]. Similar phenomenon has been observed when annealing bonded aluminum films [37].

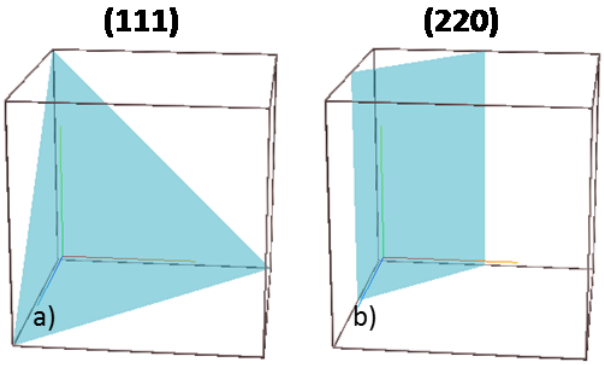

Fig. 5: Graphical representation of miller indexes corresponding to different grain orientations. a) Sputtered Cu (111). b) Annealed Cu (220)

The effect of annealing temperature on interfacial adhesion energy has been studied. Jang *et al.* found in their study that 1 h anneal at 200°C, 250°C and 300°C resulted in interfacial adhesion energies of 2.69 Jm^{-2}, 8.87 Jm^{-2}, and 12.17 Jm^{-2}, respectively. Whereas without anneal the interfacial adhesion energy was measured at 2.79 Jm^{-2}, when the bonding was carried out at 300°C using force of 25 kN in pressure of 1.33 x 10^{-3} mbar for 30 min [38]. Annealing significantly increases the interfacial adhesion

energy. At temperatures of 250°C and 300°C it was measured to be about from 3 to 4 times greater as compared to samples without annealing. Results also indicate that in low temperatures of 200°C, the annealing does not influence the bonding at all [38]. This suggests that 200°C is not high enough temperature to facilitate recrystallization. However, 250°C is not the only recorded minimum temperature higher values have been reported. Chen *et al.* found anneal to be detrimental when done at temperatures below 300°C [39]. Though the experiment did use different pre-treatment methods, the difference is still notable [38], [39].

2.3.2 Surface roughness and its effects on diffusion bonding

Surface roughness is considered to be one of the most important factors affecting the quality of thermocompression bonding of copper films [35]. As so, it deserves a closer look. Chen *et al.* have proposed three different mechanisms for bonding, based on the surface topography [35]. These mechanisms are: “peak-to-peak” where contact happens between the highest points of two surfaces of comparable roughness, “peak-to-valley” where contact occurs between the highest and the lowest points of two surfaces of similar level roughness and lastly a mechanism where the contact is between surfaces of different scale roughness [35].

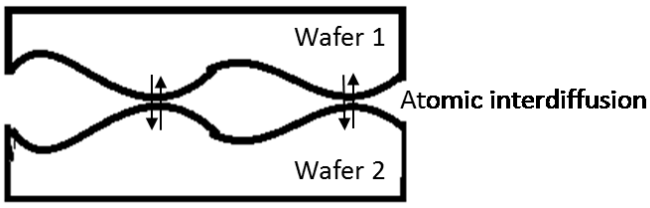

Fig. 6: Depiction of "Peak-to-peak" contact. Where atomic diffusion (indicated with arrows) between the bond interfaces occurs at the peaks of the films.

In “peak-to-peak” where the contact area is small, the distance between the two interfaces can be in atomic scale. The diffusion of Cu atoms and hence the grain growth

takes place in the contacting peaks, indicated by arrows in Fig. 6. Ultimately, the bond interface disappears and one homogenous region is formed [35].

In “peak-to-valley” conditions, the bonding mechanism is different (Fig. 7). First, the bonding force is less than in “peak-to-peak” contact; this is because the bonding interfaces are not perpendicular to the load direction of the bonding tool. In high temperature, the atoms on surface are malleable enough for the surfaces to deform and match each other. In the anneal treatment the crystal growth will occur from the wavy interface leading to distinct zigzag-type interface [35].

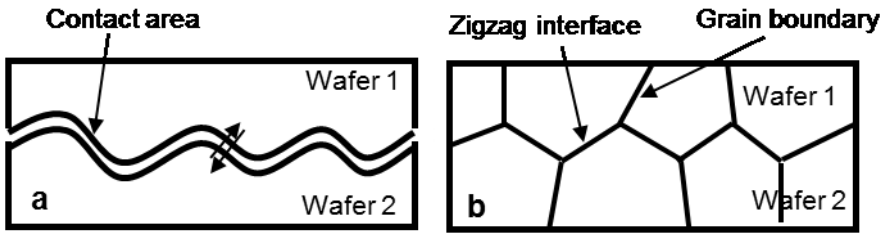

Fig. 7: "Peak-to-valley" contact. a) Contact area is not perpendicular to load, interdiffusion demonstrated with arrows. b) Grain growth results in visible grain boundaries in a zigzag pattern.

In case where the surface roughness of bonding films is of different scale, the peaks and valleys do not match during bonding. The miss matched valleys result into voids in the bond interface. However, the formation of voids can be mitigated by the use of high enough bonding force. The force will cause the layers to deform and make the smaller asperities migrate and match the valley on opposite side. This mechanism leads to a decrease in bonding energy. After bonding some voids are expected to remain in the interface, the remaining voids could be removed via crystal growth mediated by a heat treatment [35].

2.4 *In situ* oxide removal methods

In situ oxide removal methods are performed in the bonding tool. The advantage of *in situ* methods compared to *ex situ* methods is that there is no need to expose the wafers to ambient air between the pretreatment and bonding. The two most common *in situ* pretreatment methods are presented, and their effectiveness in low temperature copper thermocompression bonding is discussed.

2.4.1 Forming gas anneal

Forming gas refers to a mixture consisting of hydrogen and an inert gas. A commonly used composition of the two gasses is 5% of H_2 and 95% of N_2 [40], [41]. However, use of other inert gasses instead of nitrogen, such as helium and argon, have been reported [42], [43].

Forming gas anneal is a commonly used method for removal of oxide layer from copper bonding surface [40]. The reaction between oxidized copper and the hydrogen of the forming gas is presented in reaction equations (2) and (3) [41]. In the exothermic reaction copper(II) oxide and copper(I) monoxide are reduced with hydrogen to form water vapor and metallic copper. The reduction of CuO and Cu_2O in H_2 atmosphere takes place in temperatures above 127°C [44].

$$\mathrm{CuO_{(s)} + H_{2\,(g)} \rightarrow Cu_s + H_2O_{(g)}} \quad (2)$$

$$\mathrm{Cu_2O_{(s)} + H_{2\,(g)} \rightarrow 2Cu_{(s)} + H_2O_{(g)}} \quad (3)$$

Forming gas anneal is reported to increase surface roughness; however the increase is not severe. Fan *et al.* found the surface roughness of sputtered copper film to be around 0.95 nm immediately after sputtering and 5.89 nm after storage of five days and forming gas anneal [40].

The effectiveness of forming gas anneal in oxide removal has been determined by x-ray photoelectron spectroscopy (XPS). The O_{1s}/Cu_{2p} ratios of sputtered copper film for fresh sample, after 5 days in cleanroom air and after forming gas anneal were

measured and found to be 0.59, 0.91 and 0.58 respectively [40]. The forming gas anneal can keep the oxygen content reduced for up to the same level as deposited.

The interfacial adhesion energy was measured for a fresh sample, after 5 days in cleanroom air and after forming gas anneal using four-point bending test and the values were found to be 14.20 Jm^{-2}, 4.48 Jm^{-2} and 11.72 Jm^{-2}, respectively [40]. Forming gas anneal leads to large increase in adhesion energy for samples that have oxidized in ambient air. In oxide removal forming gas anneal is superior to acetic acid wet treatment, the adhesion energy is nearly double to that of acetic acid (6.31 Jm^{-2}) [40]. Comparison of interfacial adhesion energy values is presented in table (Table 2), the bonding was done at 250°C for 1 h using wafers with Ti (50 nm)/Cu (300 nm) bonding layer on SiO_2.

Table 2: Bond quality and surface oxygen content of different pretreatment methods. The values are from previous study by Fan et al. [40].

	Fresh	5 days	SAM	Forming gas	Acetic acid
Dicing yield (%)	97.9	44.8	96.6	78.6	72.4
Interfacial adhesion energy (Jm^{-2})	14.20	4.48	13.56	11.72	6.31
Hermeticity ($atm.cm^3s^{-1}$)	7.02×10^{-10}	1.31×10^{-9}	6.55×10^{-10}	7.58×10^{-10}	9.20×10^{-10}
O_{1s}/Cu_{2p}	0.59	0.91	0.59	0.58	0.55

2.4.2 Formic acid treatment

Formic acid, also known as methyl acid, treatment is common method for oxide removal in wafer bonding. The formic acid decomposes to H^+ and $HCOO^-$ on copper surface at room temperature. At high temperatures $HCOO^-$ decomposes further to H^+ and CO_2 resulting in formation of hydrogen absorbed on copper surface. Hydrogen then reacts with oxygen of the copper oxides producing water vapor [45]. The reactions are presented in detail in equations [46] as

$$\mathrm{HCOOH_{(g)} + O^{2-}{}_{(ads)} \rightarrow HCOO^{-}{}_{(ads)} + OH^{-}{}_{(ads)}} \quad (4)$$

$$\mathrm{HCOOH_{(g)} + OH^{-}{}_{(ads)} \rightarrow HCOO^{-}{}_{(ads)} + H_2O_{(g)}} \quad (5)$$

$$\mathrm{HCOO^{-}{}_{(ads)} + OH^{-}{}_{(ads)} \rightarrow CO_{2(g)} + H_2O_{(g)} + 2e^{-}} \quad (6)$$

where the reaction Eq. (6) occurs in elevated temperature [46]. Several minimum temperatures are reported for this reaction: 550 K ≈ 277°C [47], 150°C [45] and 400 K ≈127°C [46]. Yougns *et al.* found that formic acid will decompose to CO_2(g) and H_2(g) at around 400 K. However further increase in temperature is needed for H_2O to be formed from reaction between oxygen and both acidic and methyne hydrogen atoms instead of reaction with two acidic protons [47]. Regardless of exact temperature the copper oxides are reduced in typical bonding temperatures from 200°C to 450°C. The Eq. (6) changes the overall stoichiometry of oxide reduction (HCOOH:O_2) from 2:1 to 1:1 reducing the consumption of HCOOH [46].

Another drawback is that in Eq. (5) the formate ion remains adsorb in the Cu surface and without Eq. (6) it is not removed from copper surface. At low (≤ 200°C) surface treatment temperatures insufficient decomposition of formic acid can lead to formation of copper formate [45], [48]. In fact, Yang *et al.* found formic acid to be incapable of reducing the Cu surface at temperatures of 150°C and lower [48]. In these situations, the formic acid can be decomposed to CO_2 and H_2 with the help of Pt catalyst [49]. Yang *et al.* used Pt foil in the gas line nozzle of the bonder, to decompose the incoming formic acid [45]. After passing the nozzle, the gas had H_2 content of 0.1 %, indicating partial decomposition of formic acid into H_2 and CO_2. Use of Pt catalyst in pretreatment increased the bond shear strength from 20 MPa to 28 MPa, when bonding was carried out at 200°C using force of 1 kN for 60 min [45].

Even without Pt catalyst, successful thermocompression bonding has been achieved in low temperatures [50], [48]. Two CMP smoothened copper films with surface roughness Ra of ~2 nm were successfully bonded at temperatures as low as 150°C with 10 min formic acid treatment. Though successful, the bond was found to be weak at bonding temperatures below 200°C [48].

2.5 *Ex situ* surface cleaning and oxide removal methods

Ex situ methods are performed outside the bonding tool. The major drawback compared to *in situ* methods is that the wafers are inherently exposed to ambient air between pretreatment and bonding steps. On the other hand, there is a great deal of pretreatment methods that cannot be done in the bonding tool, such as all of the wet etching methods. The previously described *in situ* methods could be performed also *ex situ* in a furnace separate from the bond tool. A few common pretreatment methods are presented with focus on those that can be performed at VTT Micronova clean room.

2.5.1 Acetic acid dip

One surface cleaning method used for oxide removal is wet etch cleaning with acetic acid solution. In this method Cu wafers are cleaned by submerging them in acetic acid solution, dried and bonded immediately [40]. The effect of acetic acid cleaning has been studied and it was found that on wafers that have been in ambient air for 5 days the O_{1s}/Cu_{2p} ratio reduced from 0.91 to 0.55 giving a 40% reduction in surface oxide [40]. Interfacial adhesion energy for samples with acetic acid cleaning was measured to be 6.31 Jm^{-2} which is an improvement compared to a sample without the surface treatment (4.48 Jm^{-2}). However, the interfacial adhesion energy is significantly less than what is achieved using forming gas anneal (11.72 Jm^{-2}) [40].

Copper is highly resistant to corrosion in the presence of acetic acid. However, it does react with cuprous oxide (Cu_2O) and cupric oxide (CuO) [51]. This selectivity makes acetic acid well suited for copper oxide removal, when damage to underlying copper must be kept minimal. The chemical reaction between the native copper oxide and acetic acid can be presented as [51],

$$CuO_{(s)} + 2CH_3COOH_{(aq)} \rightarrow Cu(CH_3COO)_{2(aq)} + H_2O_{(l)} \quad (7)$$

$$Cu_2O_{(s)} + 4CH_3COOH_{(aq)} \rightarrow 2Cu(CH_3COO)_{2(aq)} + H_2O_{(l)} + H_{2(g)} \quad (8)$$

The specific parameter for this step are not commonly stated. Most paper refer to surface cleaning with acetic acid without giving the exact concentrations, exposure temperature or exposure time. Commonly, at least one of the three is missing. Several papers state the use of “dilute acetic acid” in oxide removal [40], giving the impression that the acetic acid solution has low concentration of acetic acid. However, Chavez and Hess have described these steps quite accurately in their study [51]. It has been found that acetic acid can only tolerate up to 4 vol. % of water without hindering the oxide removal process [51]. Calling such solution “dilute” is most definitely misleading.

Why is the concentration such a significant factor? The importance of removing water from the cleaning process lies in the fact that copper reacts with water. The three different reactions [51]:

$$Cu_{(s)} + H_2O_{(l)} \rightarrow CuO_{(s)} + H_{2\,(g)} \quad (9)$$

$$2Cu_{(s)} + H_2O_{(l)} \rightarrow Cu_2O_{(s)} + H_{2\,(g)} \quad (10)$$

$$Cu_{(s)} + 2H_2O_{(l)} \rightarrow Cu(OH)_{2(s)} + H_{2\,(g)} \quad (11)$$

These reactions are catalyzed by dissolved oxygen [51], [52]. Out of these reactions Eq. (11) happens instantly when copper is in contact with water, forming copper(II) hydroxide. For that specific reason, rinsing the sample with DI water after the cleaning step was found to be detrimental [53]. According to Chavez and Hess, the amount copper(II) hydroxide was on sample was nearly as much as prior to acetic acid treatment rendering the treatment practically useless [51]. The concentration of $Cu(OH)_2$ was calculated from XPS measurements of atomic percentage of oxygen. The percentage of oxygen was measured prior to treatment, after acetic acid treatment and after acetic acid treatment with H_2O rinse corresponding to values of 58%, 15% and 50% respectively. However, the results also show that H_2O rinse reduces the amount of Cu_2O from 19% without rinse to 10% with rinse. Chavez and Hess, while arguing on the effects of rinse for $Cu(OH)_2$, have not commented on this noticeable reduction on

Cu_2O [51]. Tu *et al.* have also studied the effect of water rinse, they found initial copper oxide layer thickness of 24.2 ± 0.3 Å to have been reduced to 0 ± 1.0 Å with only acetic acid treatment and 8.5 ± 0.6 Å with acetic acid treatment followed by H_2O rinse [53]. Based on these results saying that H_2O rinse makes the pretreatment useless is too harsh, however the rinse does hinder the overall oxide removal potential. Instead of DI-water rinse, drying with nitrogen was recommended [51], [53].

The appropriate etch times for acetic acid pretreatment have been studied. Based on XPS measurements an etch time of 5 minutes was found to be sufficient to remove the oxygen from the copper surface. Higher etch time has not been found to reduce the oxygen content of the surface any further. In fact higher etch time was noticed to lead to a decrease in interfacial adhesion energy [54]. The acetic acid pretreatment was carried out at the temperature of 35°C [54]. According to Chavez and Hess elevated temperature is not required for the reaction to occur, but instead used to keep the temperature constant across the measurements [51]. If the process were to be implemented in room temperature, a difference of approximately 15°C to reference temperature is expected to change the reaction kinetics. The change in reaction kinetics will likely alter the appropriate reaction times.

2.5.2 Hydrochloric acid dip

Hydrochloric acid (HCl) is a commonly used chemical in pretreatment of copper surfaces prior to bonding [55], [56]. Wafers are typically dipped in 1:1 (by volume) solution of HCl:H_2O, followed by DI water rinse and spin drying [55]. The method essentially works by using the hydrogen chloride to etch copper oxides. The details of reactions between HCl and both copper(I) oxide and copper(II) oxide are depicted in equations (12) and (13) respectively [39].

$$Cu_2O_{(s)} + 8Cl^- + 2H^+_{(aq)} \rightarrow 2{CuCl_4}^{2-}_{(aq)} + H_2O_{(l)} + 2e^- \quad (12)$$

$$CuO_{(s)} + 4Cl^- + 2H^+_{(aq)} \rightarrow {CuCl_4}^{2-}_{(aq)} + H_2O_{(l)} \quad (13)$$

As previously described the HCl pretreatment process includes DI water rinse after the HCl clean. This can prove to be a major drawback as copper reacts with water forming copper(II) hydroxide Eq. (11) [51]. The formed copper(II) hydroxide will inhibit the diffusion of Cu atoms across the bond interface. This could be the reason why using HCl cleaned samples at bonding and anneal temperature of 250°C had failure rate of above 20% [39]. Here the failure was defined as delamination during or after dicing. Effects of HCl cleaning on surface roughness have also been studied. The cleaning was found to increase the surface roughness of copper from 1.15 nm to 1.55 nm. This was addressed as one of the reasons for poor bond quality at low temperatures [39]. However, considering the size of the increase, less than 1 nm, it is hard to believe it to be significant. Better dicing yields (97%) can be obtained at same bonding temperature with higher surface roughness of 2.51 nm when self-assembled monolayer passivation is used instead of HCl dip [40].

2.5.3 Citric acid

At low bonding temperature of 175°C the use of 1 wt. % citric acid treatment with forming gas anneal lead to fully bonded wafers whereas using only forming gas anneal resulted in 85 % of the wafer area to be weakly bonded. Using citric acid treatment alone, lead to weak bonding in all of the wafer area [57]. Citric acid cleaning is typically applied to wafer in form of spray. One method for citric acid treatment is use of 1 wt. % citric acid diluted with DI-water on an EVG®301 single wafer cleaning system for 2x2 min after which DI-water rinse is used for particle removal [57], [43]. Impact of the pretreatment method on surface roughness has been studied. The citric acid treatment in combination with forming gas anneal was found to have only marginal effect on surface roughness of Cu film [43].

2.5.4 Self-assembled monolayer passivation

Self-assembled monolayer (SAM) passivation refers to a surface treatment method; where instead of removing the oxides from surface, the aim is to prevent the oxidation of copper altogether. This is typically done by immersing the wafer into an organic substance right after sputtering to create a protective layer on top of the copper surface [58], [59].

Fan *et al.* have used 1-hexanethiol as a protective film succeeding to improve the bond quality. Comparable results to other surface cleaning methods are presented in table (Table 2). The 1-hexanethiol was applied by immersing wafers for 3 h into 1 mM 1-hexanethiol in ethanol solution, inside a nitrogen purged dry box [40]. Removal of SAM is typically done by heat treatment in the bonding tool. 1-hexanethiol can be desorbed from the Cu surface by heating to 250°C [40]. While removal via anneal sounds handy, does the existence of SAM cause limitations on processing the wafer prior to bonding. There seem to be little research on compatibility of SAM on lithography. In lithography, wafers are typically primed with hexamethyldisilazane (HMDS) at elevated temperatures to ensure proper adhesion of photoresist [60], [61]. The hydrophobicity of SAM layer can be problematic in wet etching.

During SAM passivation the thiol group binds to Cu surface while the hydrophobic methyl group is oriented away from the surface. The underlying mechanism for the SAM passivation lies in preventing contact between surface and moisture via hydrophobic layer [58], [59]. Hence, the effectiveness of thiol based SAM passivation was found to be directly proportional to carbon chain length. Stronger intermolecular forces, resulting from longer chain length, cause the better hydrophobicity. However, the increase in intermolecular forces can also be detrimental for the overall process. Desorption of SAM via anneal becomes increasingly difficult the stronger the intermolecular forces become [58].

2.6 Copper microstructure fabrication methods

A short overview is given to microfabrication methods used in fabrication of copper structures. Explaining the theory behind lithography, electrodeposition and etching, as well as introducing a few common etchants for copper.

2.6.1 Lithography

Photolithography typically consists of three steps: resist coating, exposure and development. However, prior to resist coating the wafers are typically primed. In priming, the wafers are coated with a hydrophobic monolayer that increases resist adhesion. Hexamethyl disilazane (HDMS) vapor is commonly used as a primer [62].

The resist coating itself is done via means of spin coating, which is the standard application method. Small amount of resist is poured to slowly rotating or stationary wafer. Next, the wafer is spun and due to law of continuation excess resist thrown out of wafer surface [62]. The thickness of remaining resist layer is dictated by the rotation speed of the wafer, typically between 1000 rpm and 8000 rpm, and the viscosity of the resist [63]. Resist coating can also be applied by other means, such as electrochemical coating, casting and spray coating, although these methods are not as common as spin coating [62].

In exposure ultraviolet light (UV) is radiated trough a mask on to the resist. Mask covers selected areas of the wafer, so that only desired areas of the resist are radiated. The UV radiation changes the chemical structure of the photoactive component of the resist, diazonapthoquine in most positive resists [62]. After the UV exposure, the photoresist is developed by immersing it in developer solution. If positive resist was used the exposed area is dissolved in the developer, where as in case of negative resist the developer dissolves the unexposed areas. There is also a third type of resist, known as image reversal resist, which is essentially a positive resist that can be polymerized, using elevated temperature, into a form that is not soluble in developer. In other words, it can be used in either polarity [64].

2.6.2 Electrodeposition

Copper microstructures can be fabricated by electroplating from copper seed layer in pattern determined by photoresist. In electrodeposition, direct current is used transfer copper ions from the electrode onto a wafer [65]. Commonly an aqueous solution is used to allow transport of ions to wafer, the transport mechanism can be controlled with other molecules and ions in the solution.

A typical electrolyte bath contains copper sulfate, sulfuric acid and various additives. These additives can be divided into accelerators, suppressors and levelers [66]. Accelerators, such as organic disulfides, are used to increase the deposition of copper in desired areas whereas suppressors, such as polyethylene glycol, are used to inhibit the deposition in unwanted regions [67]. Levelers are used to polarize areas with high current densities to even out the current distribution, and making deposition uniform [66].

2.6.3 Copper etchants

In fabrication of copper microstructures a common method is to pattern a blank copper wafer by selectively covering it with photoresist and removing the material from unprotected areas via etching. Several etchants for Cu have been recorded in literature. A few common ones are Cu $FeCl_3$ 200 (30% $FeCl_3$ + 3-4% HCl + H_2O) and Cu APS 100 (15-20% $(NH_4)_2S_2O_8$ + H_2O) with etch rates of 3900 nm min^{-1} and 2500 nm min^{-1} respectively. Both of the etchants can be patterned with photoresist [68]. Cu $FeCl_3$ 200 is recommended to be rinsed in a 5-10% HCl solution after etching. The overall reaction for $FeCl_3$ based etchants is presented in Eq. (14). The $FeCl_3$ can further react with CuCl to create $CuCl_2$, which is also copper etchants, which reacts with Cu leading back to CuCl [69].

$$\mathrm{FeCl_3 + Cu \rightarrow FeCl_2 + CuCl} \tag{14}$$

The effects of $FeCl_3$ based etchants on surface roughness have been studied. Using 3.76 M $FeCl_3$ solution at 50°C the surface roughness R_a was measured to be 1.92 µm

whereas using $CuCl_2$ based etchant gave roughness of 0.73 µm [69]. The roughness values were recorded every 5 minutes, and the presented values were obtained after surface roughness had stabilized. For some reason, Cakir *et al.* have not reported the surface roughness of copper prior to etching [69].

Another copper etchant is sodium persulfate but less research can be found on this etchant as compared to the previously mentioned etchants. One method of applying persulfate is in etch solution of sulfuric acid, persulfate, imizole, water and amidosulfuric acid [70]. Sodium persulfate has been used in etching of copper in printed circuit board fabrication. Persulfate-type microetchants are recorded to attack the grain boundaries of the copper, creating a rough surface [71]. The recorded etch rate for sodium persulfate is 0.38-2.03 µm min^{-1} for concentrations of 72 g l^{-1} to 300 g l^{-1} [71].

2.7 Bond area geometry

Seal ring is a copper microstructure that surrounds the MEMS device in the wafer plane. When two seal rings are bonded, a cavity is formed inside the seal ring. The significance of the geometry and line width of seal ring has been studied, focusing on the dependency of hermeticity on seal ring structure as well as long-term stability. In one such study, Fan *et al.* have researched the importance of seal ring width in regards to hermeticity of sealed area [72]. With bonding in 300°C, even at line width of 5 µm excellent leak rates of 1.3 x 10^{-9} atm. cm^3 s^{-1} were obtained. This is an order of magnitude lower than the reject limit, 5 x 10^{-8} atm cm^3 s^{-1}, defined by MILSTD-883E standard [73].

The reliability of hermetic sealing was tested by means of temperature cycling test, humidity test with different storage levels and corrosion in acidic/basic environment. In temperature cycling test the wafers were subjected to temperature changes form -40°C to 125°C, for up to 1000 cycles. After 1000 cycles even the narrowest seal ring with width of 5 µm didn't suffer significant losses in hermeticity, maintaining below standard leak rate [72]. Fan *et al*. have also studied the effect of humidity on reliability of hermetic sealing [72]. The leak rate had no significant change even at highest

humidity level described by IPC/JEDEC J-STD-020C standard, which is 168 h in relative humidity of 85% at 85°C [74]. Sufficient hermetic stability was achieved at line width of 10 µm, after that point the resistance to humidity is independent of line width [72].

On terms of geometry Fan *et al.* have studied the difference between single and multiple ring design in terms of hermetic sealing [75]. Leak rate of single 50 µm compared to double 20 µm ring when bonded at 300°C was about the same, around 5 x 10^{-10} atm cm^3 s^{-1}. However, when bonded at 250°C the leak rate on the double ring was around 3 x 10^{-10} atm cm^3 s^{-1}, whereas the single ring structure had average leak rate 1.9 x 10^{-9} atm cm^3 s^{-1}. In addition, the standard deviation between helium leak rate measurements was a lot smaller on double ring structure compared to single ring design [75]. Malik *et al.* have studied the impact of having rounded corners on square shaped seal rings [76]. In gold thermocompression bonding there was no significant difference in bond strength between sharp and rounded corners.

2.8 Wafer alignment

There are four major wafer alignment methods in wafer bonding. These are top side alignment, infrared alignment, backside alignment (also known as bottom side alignment) and inter-substrate alignment [18]. Due to technical limitations of the available equipment only infrared and backside alignment are examined in detail.

IR-alignment is a bond alignment method based on illumination of alignment marks using infrared light. In IR, the alignment marks are on bond interface and IR source radiates through the wafer pack. Key requirement is that the substrates are transparent to IR-radiation [18], like silicon [77]. In general, wafer inspection tools use IR-radiation around 1 µm [78]. For example, existence of IR absorbing metal films will prohibit the use of the method. The method requires use of double side polished wafers, as the backside roughness of standard wafers reduces image quality due to scattering [18]. In addition high doping and thickness of wafer interfere with IR radiation.

In bottom side alignment, two wafers are aligned by fitting the alignment marks on the backside of bottom wafer to the alignment marks on the front side of the top

wafer. This is typically done by taking a digital image of the alignment marks on top wafer after it has been loaded into the alignment tool. The alignment marks on the back side of the bottom wafer are then aligned to match the digitalized image. Alternatively the alignment can be done using bottom wafer that is transparent, in that case image of the top wafer is not required since both alignment marks are visible simultaneously [18].

2.9 Characterization methods for bonded wafers

A general overview is given on typical characterization methods of bonded wafers. Those characterization methods that are well known in MEMS industry, such as scanning electron microscopy (SEM) are not explained here.

2.9.1 Scanning acoustic microscopy imaging

Scanning acoustic microscopy (SAM) imaging is one of the few nondestructive methods for determining the bond quality. It is a commonly used method for characterizing the bond interface and determining the existence of micro-voids (< 1 µm) [79]. As the name suggests, the measurement is based on studying the behavior of a sound wave. A typical SAM instrument consist of an acoustic generator, two acoustic lenses, water cell, sample holder, mechanical scanning system, acoustic detector and signal processing electronics. The instrument functions essentially by emitting a focused acoustic beam and detecting the reflected, refracted and scattered signal from the boundaries where variations in the elastic parameters exist [80].

From the shape and size of the voids observed with SAM, the type of wafer bonding failure can be determined. For example, small perfectly round voids are likely caused by particle contamination [81]. Whereas, interfacial outgassing can lead to round shaped voids of various sizes. Interfacial outgassing refers to gas generated at bond surface that is trapped between the wafers [81]. One source for outgassing can be sublimation of SAM layer [58]. Other causes for voids are organic contamination, wafer bow and issues with flatness and micro-roughness of bonded surfaces.

2.9.2 Bond strength

There are several different methods for determining the bond strength between two wafers. The most common of these are the four-point bending test, the razor test, the tensile test and the shear test. All four previously mentioned methods are described with focus on tensile and shear testing.

In four-point bending test the one side of the silicon wafer is notched to a depth of 400 µm. Force is the applied form two points on the opposite side of the wafer. The schematic of the four-point bend test apparatus is shown below (Fig. 8). Using the test, interfacial adhesion energy between weakly bonded thin films can be measured (15) [54]. The interfacial adhesion energy G can be solved from:

$$G = \frac{21(1-\nu^2)\,P^2L^2}{16Eb^2h^3} \tag{15}$$

where v is Poisson's ratio, E is the elastic modulus of the material, P is measured load, L is distance between inner and outer loading points and b and h are the sample width and thickness, respectively [82].

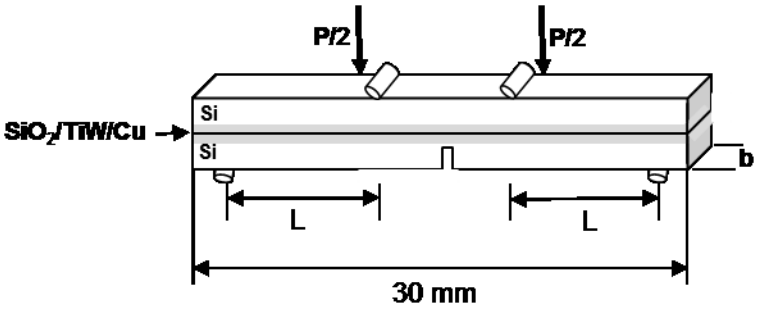

Fig. 8: Schematic drawing of four-point bend test setup. Load is applied downwards to cause a crack at the notch.

Another method for determining bond strength is the razor test. There are a couple of different variants on razor testing, but generally a razor blade is pushed between

the wafers and the propagation of the crack starting from the tip of the blade is monitored. The weaker the bond strength the further the crack advances. Razor test can be used to test the bond strength qualitatively, where bonding is considered good if the blade cannot penetrate the bonding interface [56].

In the tensile test, the diced sample is typically mounted to pull studs via gluing and force is applied to the sample perpendicular to bond interface [83], [84]. The force applied to the sample is steadily increased and the maximum force that the sample can withstand before breakage is recorded. From the force, the breaking pressure is calculated using the area of the bonded structure [85]. The glue used in sample preparation, as can be observed from the drawing (Fig. 9), limits the applied force. One other drawback of gluing is that the sample preparation will take more time compared to the other methods and two single use pull studs are consumed for every measurement.

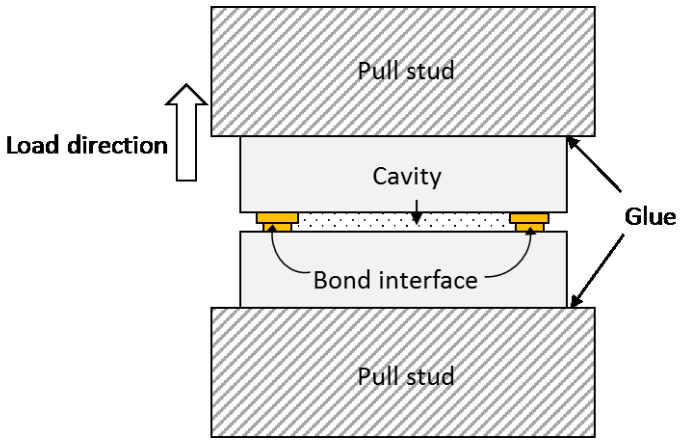

Fig. 9: Schematic drawing of a tensile test setup, where sample is glued into pull studs. Top pull stud is pulled away from the bottom one and load is transferred to bond interface.

It is recommended to use samples with defined bond area surrounding a cavity [86]. While samples diced from blank bonded wafers can be used, they are more prone to

voids and edge defects resulting from dicing. These defects can act as cracks, influencing the results. Typically blank wafers have higher variance between samples [86]. In previous research tensile strengths between 200 MPa and 310 MPa have been recorded for Cu thermocompression bonding at bonding temperature of 300°C, depending on the surface treatment used [87]. Far lower bond strength values for copper have also been reported. Chen *et al.* have reported tensile strengths of 32 MPa, 27 MPa and 14 MPa for wafers bonded in 300°C, 250°C and 200°C, respectively [88].

MIL-STD-883E standard (METHOD 2031.1) describes a flip-chip pull-off test. The bonding is considered as a failure if the pull results in a failure under applied stress less than 500 kg/in^2 x average solder bump area (in^2) x number of solder bumps [73]. In SI units, this corresponds to approximately 7.6 x 10^{-6} N µm^{-2} that is 7.6 MPa.

Shear testing is similar to tensile testing, in that the measured quantity is the breakage force. However, unlike in tensile test here the force is applied in parallel to the bond interface [89]. In shear testing the sample preparation is typically easier, chips do not need to be glued, but are placed into a specific jig [84]. A typical setup for shear test is presented in schematic below (Fig. 10).

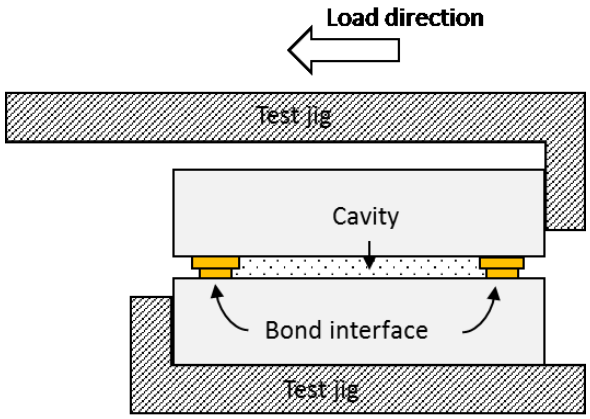

Fig. 10: Schematic drawing of a shear test setup. The test jig applies force to the top and bottom wafer of the sample, in direction parallel to the bond interface.

Chen et al. have reported bond strength for thermocompression bonded copper at different bonding conditions [88]. Shear forces of 25 kgw, 21 kgw, 15 kgw for samples bonded at 300°C, 250°C and 200°C. For some reason the results were presented in obscure units of kgw (kilogram weight), when translated to SI units they correspond to 9.8 MPa, 8.2 MPa and 5.9 MPa for samples bonded at 300°C, 250°C and 200°C, respectively [56], [88]. The samples were diced from blank bonded wafers. As a reference, thermocompression bonding aluminum (Al/Sn/Al/Sn/Al//Al/Sn/Al/Sn/Al) at 360°C or 380°C gives strength of 52.2 ± 37.8 MPa for hermetic die [90]. For gold-tin eutectic bonding shear strength above 51.7 MPa has been recorded, though in the article the failure did not occur at the bond interface [17]. Hence, the stated value of 51.7 MPa is only minimum and the actual bond strength is higher.

The shear force requirements for the chip to with stand before breaking are described in MIL-STD-883E standard (METHOD 2019.5) [73]. For the chip sizes used in this work, the minimum strength required by standard is 400 kg/in^2 the area is the bond area of a chip, in SI unites this relates to approximately 6.08 MPa.

2.9.3 Hermeticity test

Hermetic testing is used to quantify the quality of bonding from the point of view of airtightness. Commonly hermetic testing is done according the MIL-STD-883E method 1014.9 standard [75]. Said hermetic testing method is made up of two steps: helium bombing and helium leak rate detection. In the first step samples are exposed to Helium gas for 2 h, at pressure of about 0.52 MPa. In the second step the samples are taken from the bombing chamber and the helium leak rate is measured using a mass spectrometer. The MIL-STD-883E standard sets the reject limit for helium leak rate at 5 x 10^{-8} atm. cm^3 s^{-1} [73]. In other words, samples with leak rates below said value are considered hermetically sealed.

Effect of bonding temperature in Cu thermocompression on hermeticity has been studied [91]. Fan et all. found the helium leak rates to be below standard for wafers bonded at 250°C, 300°C and 350°C, with leak rates recorded at 9.65 x 10^{-10}, 7.39 x 10^{-}

^{10} and 3.98 x 10^{-10} atm. cm^3 s^{-1} respectively [91]. In other words, hermeticity of all three samples was two orders of magnitude better than the MIL-STD-883E standard reject limit.

2.9.4 Surface roughness

As previously discussed, surface roughness plays a vital role in diffusion of atoms from one bond interface to another. There are several methods for surface roughness measurements, out of which contact and optical profilometer are best known. In contact profilometer a stylus is dragged along the sample surface and the vertical movements of the stylus are measured. Where as in optical profilometer light is used instead. There are several method for determining the surface topology from reflected light such as optical interference, focus and phase detection, and projecting a pattern onto the optical image [92].

Out of these two profilometers higher accuracy can be obtained with optical profilometer as its vertical resolution can be on the order of several angstroms [93]. On the other hand, optical profilometer is restricted to optically reflective materials, whereas contact profilometer is not.

3 Experimental

Following chapter describes the sample fabrication methods used in the thesis in detail. The analysis methods and data processing are presented. Closer look is taken into pretreatment process and bonding parameters.

3.1 Structure of samples

In the thesis, thermocompression bonding blank and patterned copper films were studied. The copper film on blank wafers (Fig. 11a) was fabricated either by sputtering or by electrodeposition on sputtered seed layer. Three different methods (Methods 1-3) were used for fabrication of patterned structures. They were all used to produce a similar structure (Fig. 11b) which comprised of Cu seal rings with line widths of 60 µm to 100 µm.

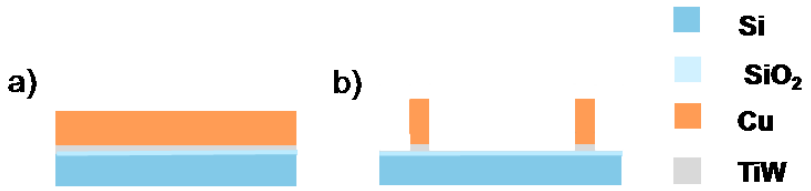

Fig. 11: Cross-sectional depiction of wafers used in the bonding experiments. a) Blanket Cu wafer. b) Patterned wafer.

3.2 Measurement series

First series of measurements was carried out using blanket Cu coated wafers and is shown in Table 3. The purpose of the measurement was to determine the minimum bonding temperature for bonding of plank, electrodeposited, wafers. A point of interest was the existence of a distinct bond interface after bonding. Due to limitations

in available equipment one pair of wafers was sputtered using Sputtering system Mark IV instead of sputtering system von Ardenne.

From these wafers, the bonding area was determined using SAM and the existence of distinct bond interface was inspected by SEM cross-sectional imaging. Distinct bond interface indicates insufficient diffusion between bond interfaces and thus lower quality bonding. Hence, finding the lowest bonding temperature where the bond interface is not visible is essential. The bonding was done in vacuum environment using force of 40 kN (bonding pressure 2.6 MPa) over 60 min.

Table 3: Samples of first measurement series. All wafers were bonded in vacuum environment using bonding pressure of 2.6 MPa over 1 h.

Sample	Sputter	Surface	Pre-treatment	Temperature (°C)	post-anneal
11/12	Mark IV	plated†/plated†	Acetic acid, H_2/N_2 anneal	400	60 min at 300°C
13/15	VA	plated†/plated†	Acetic acid, H_2/N_2 anneal	300	60 min at 300°C
18/20	VA	plated†/sputtered‡	Acetic acid, H_2/N_2 anneal	250	60 min at 250°C
21/29	VA	plated†/sputtered‡	Acetic acid, H_2/N_2 anneal	200	-
16/23	VA	plated†/sputtered‡	H_2/N_2 anneal	300	60 min at 300°C

† Bonding layer was fabricated by electroplating 1 µm copper on 300 nm Cu seed layer. ‡ Sputtered 1µm bonding layer.

In second series of measurements, electrodeposited patterned wafers, fabricated via Method 1, were bonded to blank sputtered wafers. Interest was targeted towards the surface topography of the patterned wafers, the effect of bonding pressure on formed bond structure was studied as well as the effect of used tooling and processes on the topology of copper structures.

Table 4: Second series of measurements. All electroplated wafers were fabricated using Method 1. All wafers were bonded in a vacuum environment over 60 min.

Sample	Surface	Pre-treatment	Pressure (MPa)	Tempera-ture (°C)	Anneal
17/24	plated† /sput-tered‡	Acetic acid, H_2/N_2 anneal	1.92	300	-
28/37	plated†/sput-tered‡	Acetic acid, H_2/N_2 anneal	2.37	300	-
26/38	plated†/sput-tered‡	Acetic acid, H_2/N_2 anneal	4.01	250	60 min at 250°C
27/39	plated†/sput-tered‡	Acetic acid, H_2/N_2 anneal	10.7	250	60 min at 250°C

† Bonding layer was fabricated by Method 1. ‡ Sputtered 1µm bonding layer.

The third series of measurements, consisted of bonding tests on wafers fabricated using methods 2 and 3. Glass wafers, indicated by letter G in front of sample number, were bonded to silicon wafers.

The purpose of the series was to establish a wafer level packaging process for a MEMS mirror requiring a glass cap. The glass cap had thermal limitation of 250°C, due to its antireflective coating. In the measurements the effect of fabrication method, etch solution, pre-treatment, bonding temperature and post-bonding anneal on bond strength and dicing yield was studied. The roughness of bonding surface was determined from samples 47, 48, 49 and 50 by optical profilometry.

Table 5: Measurement series 3, where all wafers were bonded in vacuum environment using bonding pressure of 19.8 MPa over 1h.

Sample	Fabrication method	Etch	pre-treatment method	Bonding Temp. (°C)	Anneal
42/G7	Method 2	H_3PO_4	10% Acetic acid, H_2O rinse, spin dry	300	no
44/G11	Method 2	H_3PO_4	10% Acetic acid, H_2O rinse, spin dry	250	no
45/G8	Method 2	H_3PO_4	10% Acetic acid, H_2O rinse, spin dry	200	no
46/G9	Method 2	H_3PO_4	99.8% Acetic acid, N_2 blow dry	250	no
47/G12	Method 2	H_3PO_4	99.8% Acetic acid, H_2O rinse, spin dry	250	no
48/G14	Method 2	$Na_2S_2O_8$	99.8% Acetic acid, H_2O rinse, spin dry	250	no
49/G16	Method 3	H_3PO_4	99.8% Acetic acid, H_2O rinse, spin dry	250	no
50/G17	Method 3	$Na_2S_2O_8$	99.8% Acetic acid, H_2O rinse, spin dry	250	no
51/G26	Method 3	$Na_2S_2O_8$	99.8% Acetic acid, H_2O rinse, spin dry	250	60 min at 250°C
52/G28	Method 3	$Na_2S_2O_8$	99.8% Acetic acid, H_2O rinse, spin dry	200	60 min at 250°C

In fourth series of measurements, depicted below (Table 6). The optical transmittance of the anti-reflective coating (AR-coating) was determined. The purpose of this series was to verify that the AR coating had not been damaged by the bonding process. Borosilicate glass (Borofloat® 33 form Schott) with and without AR-coating were used.

Table 6: Measurement series 4, samples prepared for measuring the optical transmittance.

Sample	AR coating	Thermal treatment	Bonding structures
1	No	No	No
2	Yes	No	No
3	Yes	200°C	No
4	Yes	250°C	No
5	Yes	No	Yes, Front side
6	Yes	No	Yes, Backside

3.3 Sample fabrication

A large portion of the work was spend on fabricating the wafers needed for bonding. Several problems arrived during the processing of the wafers, resulting in use of multiple processes. Each process step of three sample-fabrication-methods are described as well as the pre-treatment and bonding setups.

The use of multiple methods in the project resulted from limitations caused by the available laboratory instruments. More precisely from the mask polarity of the available masks. The overall process

The schematic for Method 1 (top down) is presented in Fig. 12. The Method 2 (bottom up) was used as the mask polarity did not allow the use of Method 1. The main difference between the Methods 1 and 2 is that in Method 1 the pattern is formed by etching down from the desired structure height, where as in Method 2 the structures are formed bottom up by electrodeposition through a resist mask. The third method (Method 3) is similar to Method 1, however, instead of using positive resist image reversal resist was used. Process flow of the Methods 2 and 3 are depicted in Fig. 13 and Fig. 14 respectively.

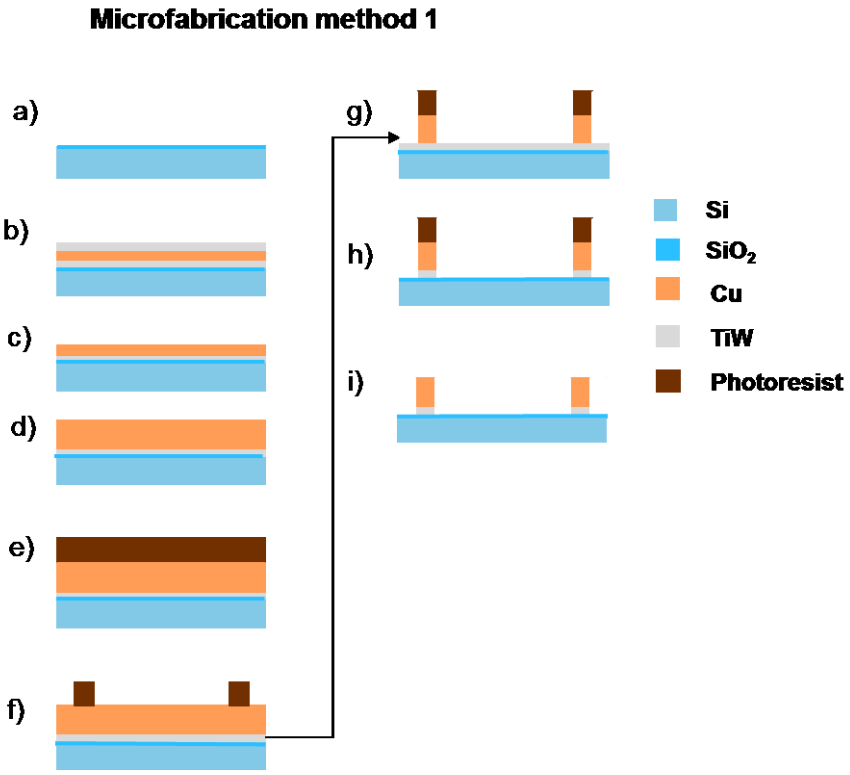

Fig. 12: Process schematic for patterned wafer fabrication by Method 1. a) Thermally oxidized Si wafer. b) Sputtering of TiW adhesion layer, Cu layer and TiW protective layer. c) Etching of TiW prior to electroplating. d) Electrodeposition of Cu. e) Spin coating the wafer with AZ9260 photoresist. f) Exposure and development with AZ400K developer and resist trimming with Oxford PRS 900 plasma stripper. g) Etching copper with HNO_3 and H_3PO_4 based etchant. h) Etching TiW adhesion layer. i) Resist removal using solvents and posistrip.

3.4 Sputtering and electrodeposition

The sputtering was done using Von Ardenne CS730 S sputtering system. In the sputtering program, substrates were pre-cleaned *in-situ* with etching by means of quasi-neutral plasma beam (ISE 200 Inverse Sputter Etcher). After which, both metals were deposited using direct current mode. Titanium tungsten seed layer was sputtered on single side polished (SSP) silicon wafers with a 500 nm thermal oxidation layer. Copper was sputtered on top of the TiW seed layer. Two different thicknesses of Cu film

were deposited. On one set of wafers, 1000 nm of Cu was sputtered, whereas on another a layer of 300 nm thick sputtered Cu was followed up by 10 nm protective TiW film. The purpose of TiW protective layer was to prevent oxidation of copper in ambient air prior to electrodeposition.

The electrodeposition was done using RENA EPM 201 F by RENA Technologies, which is a manual fountain type electroplating tool [94]. Prior to electrodeposition the TiW layer was removed by wet etching and the wafers were wetted with dilute nitric acid solution. The exact electrodeposition parameters are presented in Appendix (3). Electrodeposition step is presented in schematics in Fig. 12d for Method 1 and Fig. 13g Method 2.

The motivation for fabricating the Cu layer by electrodeposition is that compared to sputtering the cost in euros per nm of film thickness is cheaper. Also the deposition time for thick films is shorter, which increases the process throughput.

3.5 Lithography

The resist coating was done using SUSS MicroTec Gamma automatic coat/develop cluster [95]. The tool was used for following steps: priming the wafers with HMDS, spin coating them with photoresist, edge bead removal, backside rinsing and baking the wafers. Out of the process steps edge bead removal was less common. In edge bead removal after spin coating the wafer was spun and a narrow jet of solvent was used to remove resist a selected distance from wafer edges. The purpose of this step was to ensure a good contact between the copper seed layer and the electroplating tool.

The before mentioned step is presented in Fig. 12e and Fig. 13c. For Method1 recipe: Q-C-NIC-6in-R3-7µm-Pr-NEBR was used and for Method2 (Fig. 13) a similar recipe, but with edge bead removal was used (Q-C-NIC-6in-R3-7µm-Pr-EBR). The detailed parameters of both recipes are listed in Appendix 3. The resist coating was done using Micro Chemical's AZ9260 positive photoresist.

After the resist coating, the wafers were kept in ambient air for 30 min before exposure, to allow solvent evaporation. The coated wafers were exposed using MA/BA6, which is a high-precision mask and bond aligner from SUSS MicroTec [96]. The exposure mode and parameters can be found in appendix (3) [97]. The photoresist was developed by immersing the wafers in diluted developer, depicted as step f) in Fig. 12 and d) in Fig. 13. For AZ9260 resist, the AZ400K was used as developer. After development, wafers were rinsed and spin-dried [97].

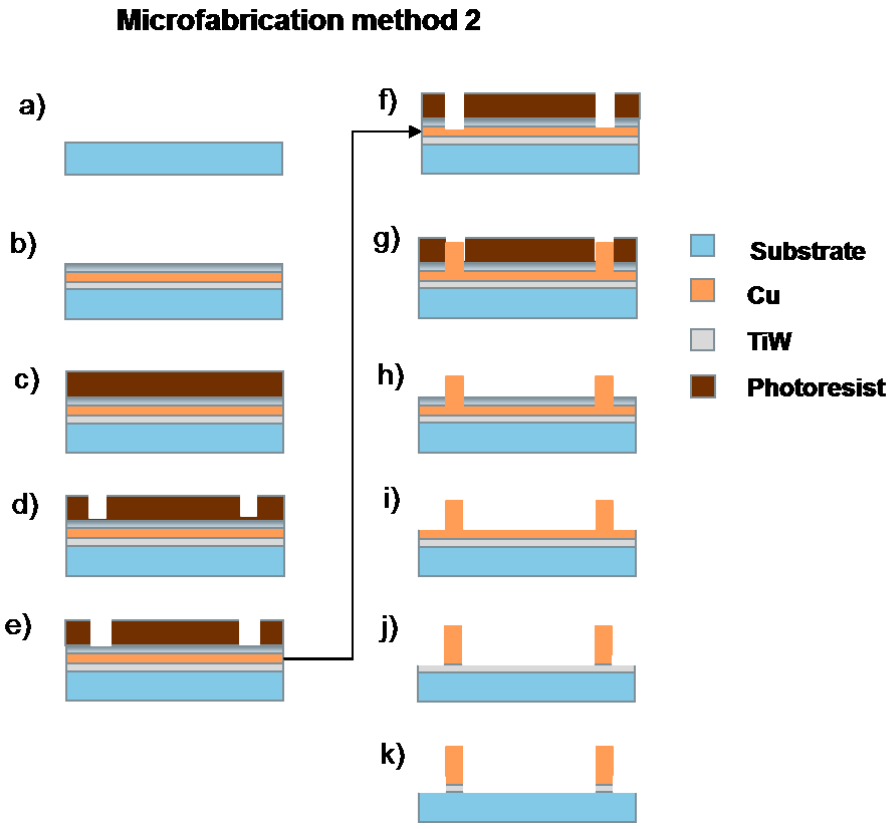

Fig. 13: Process schematic for patterned wafer fabrication by Method 2. a) Substrate b) Sputtering of TiW seed layer, Cu layer and TiW layer. c) Spin coating with AZ9260 photoresist. d) UV exposure and development with AZ 400K developer. e) Trimming the resist. f) TiW etching and HNO_3 wetting. g) Cu electrodeposition h) Solvent resist removal and resist stripping. i) TiW etching. j) Cu etching. k) Etching TiW seed layer.

Unlike Methods 1 and 2 the Method 3 uses image reversal resist instead of positive resist. This complicates the lithography process. The fabrication method is presented in Fig. 14, from the schematic, we can find lithography taking place in steps c-g. In Fig. 14c the wafer is spin coated with AZ 5214E, after which it is exposed to UV through a mask. After the exposure the resist is "reverse baked" on hotplate at 115°C (Fig. 14e), during heating the exposed resist polymerizes making it insoluble in developer. Next, the whole wafer is exposed to UV light in flood exposure (Fig. 14f), resulting in all of the exposed areas (that are not polymerized) to dissolve in Micro Chemicals AZ 351B developer (Fig. 14g).

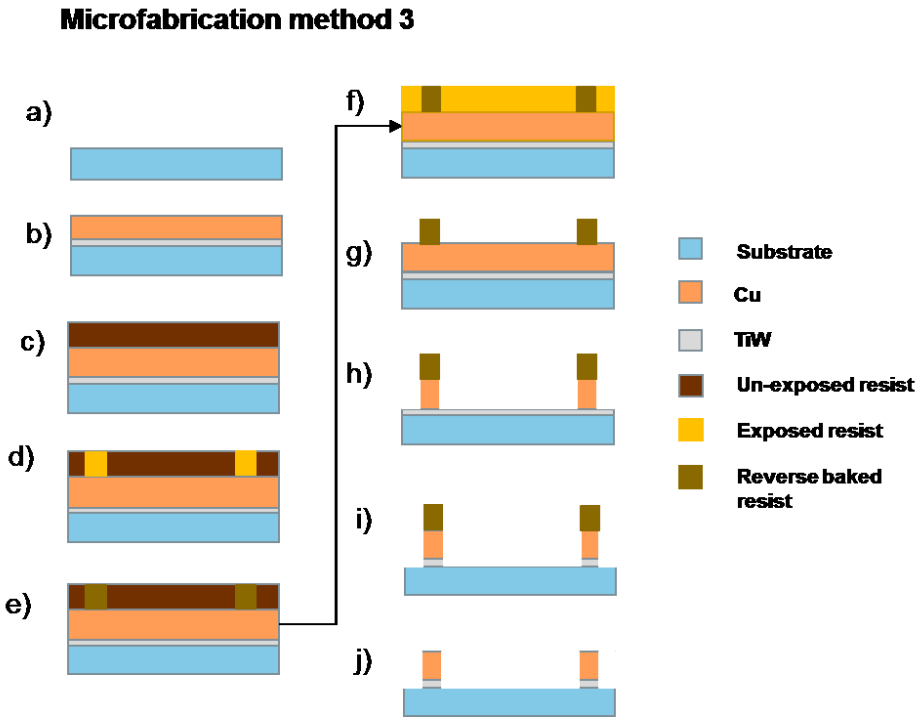

Fig. 14: Process schematic of microfabrication Method 3. a) Substrate b) Sputtering of TiW seed layer and Cu layer. c) Spin coating the wafer with AZ 5214E photoresist. d) Exposure to UV with mask. e) Reverse baking the wafer on hotplate. f) Flood exposure (no mask) to UV. g) Development with AZ 351B developer. h) Patterning of Cu by wet etching. i) Etching TiW adhesion layer. j) Resist removal using solvents and posistrip.

3.6 Plasma stripping and resist removal

In wet processes, the solution must be in contact directly with the Cu film. Therefore, plasma stripping was used to remove any resist residue from Cu surface that had not dissolved in developer. In the process flow schematic of Fig. 12, plasma stripping occurs at step f) and in Fig. 13 at step e). Two tools were used to perform the step; those were Oxford PRS 900 plasma stripper and Oxford Plasmalab 80 Plus, both from Oxford Instruments.

The plasma strip was carried out using previous VTT's process instructions [97]. However, the elevated operating temperature of PRS 900 plasma stripper caused the photoresist to deform, which lead to problems in further processing of wafers. When Plasmalab 80 Plus at RT was used in O_2-strip mode, no deformations were observed. Hence, the Plasmalab 80 Plus was used for the remaining samples.

In the resist removal (Fig. 12i), (Fig. 13h) and (Fig. 14j), the photoresist was removed from the Cu surface first via use of solvents and then with Posistrip. In the solvent resist removal the wafers were submerged in successive acetone (2x) and i-propanol bath with ultrasonic agitation. After solvent resist removal the wafers were rinsed with DIW and spin dried [97]. The last photoresist remains were removed by submerging the wafers into heated process tank containing EKC 830 POSISTRIP from EKC Technologies. The posistrip is a solution of N-Methylpyrrolidone and 2-(2-Aminoethoxy)Ethanol [98]. It is known to corrode copper in the presence of water emphasizing the need of proper drying of wafers after rinsing. The effects of Posistrip treatment on surface roughness of copper were studied.

3.7 Etching

Wet etching was used to remove unwanted regions of the metal films from the wafer. The Cu and TiW layers were removed separately with their own specific etches. The Cu-etch was not found to corrode TiW. However, according to literature the TiW etch

used does corrode copper and forms insoluble reaction products on the copper surface [99].

According to process Method 1, the patterning was done by etching the copper from unwanted areas with help of a resist mask. In other words, only defined areas of the wafer surface are exposed to the etchant. In the Method 2, the desired structures are grown by electroplating through resist mask, and etching is used to remove only the sputtered un-patterned Cu seed layer. The etching of the seed layer is done after resist removal, so in the Method 2 the whole wafer is exposed to the etchant. Therefore, the copper structures are also etched. However, as the fabricated Cu structures are several times thicker than the seed layer, they are still visible after the seed layer has been completely dissolved.

Several etchants were used in the etching of copper. The first was hydrogen peroxide activated orthophosphoric acid based etchant. Little previous research has been reported on the use of orthophosphoric acid to etch copper. A previous study found H_3PO_4-H_2O_2-H_2O solution to be suitable for etching germanium producing smooth and uniform surfaces [100]. A similar solution has been previously used at VTT for etching Cu and the component chemicals were readily available. A second Cu etchant, sodium persulfate ($Na_2S_2O_8$) was also tested. The etch solution was prepared by dissolving $Na_2S_2O_8$ in H_2O; the concentration was 100 g l^{-1}.

The top layer TiW and the seed layer TiW were etched using H_2O_2-NH_3-H_2O solution. The solution has been previously used at VTT for wet etching TiW. Hydrogen peroxide and ammonium hydroxide based TiW etch solutions are commercially available, however, the concentrations differ from the solution used at VTT [101].

As one of the wafer alignment methods required backside alignment marks, they needed to be etched on the backside of the wafer. Hence, lithography was done on the backside of the wafer and the thermally oxidized surface was etched using inductively coupled plasma advanced oxide etcher (ICP AOE) from Surface Technology Systems Plc. (STS).The etch chemistry consisted of a mixture of SF_6 and O_2.

The backside alignment marks were etched into the silicon under the SiO_2 layer using Advanced Silicon Etcher (ASE) from STS. Advanced silicon etching is a deep reactive-ion etching technique where alternating cycles of etching plasma (SF_6) and passivation gas (C_4F_8) which forms a sidewall passivation polymer, that is used to control the anisotropy of the etch process, commonly known as the Bosch process [102].

3.8 Characterization methods

Before bonding the surface roughness of the bond structures was determined. After bonding the wafers were characterized using scanning acoustic microscopy, scanning electron microscopy. The bond strength was determined by measuring the maximum shear force.

3.8.1 Surface roughness measurement by optical and contact profilometry

After surface oxidation, the surface roughness of the bonding interfaces is the second most important parameter of bonding materials in copper thermocompression bonding [35].

Surface roughness was measured using Bruker Optical profilometer Contour GT-X (hence forward known as Contour). Thera are two modes in which the tool can be used VSI and PSI. Of these the Phase-Shifting Interferometry (PSI) is the more accurate measurement, but it is only suited for surfaces with roughness less than 30 nm. As the measured surfaces are rough and the wafers have structures on them the Vertical Scanning Interferometry (VSI) mode was chosen [103]. For selected wafers the surface roughness was measured after the photoresist was removed. A contact profilometer Veeco Dektak V200Si was used in confirming the surface roughness measurements. However, the outdated data output format of the tool limited its usefulness.

3.8.2 Bond quality characterization by scanning acoustic microscopy

Scanning acoustic microscopy (SAM) was used to determine the bond quality of bonded wafers. Measurement were performed with Sonix HS3000 Acoustic microscope which is capable to detect voids with diameter greater than 10 µm [104].

The size of bonded and non-bonded area was determined via computational analysis of SAM images. The percentage of the successfully bonded wafer area was determined from the SAM images as follows: edge exclusion was excluded, the image was segmented by color, the remaining white non-bonded area was divided by total wafer area (black and white). The SAM image before and after image data processing is shown in Fig. 15.

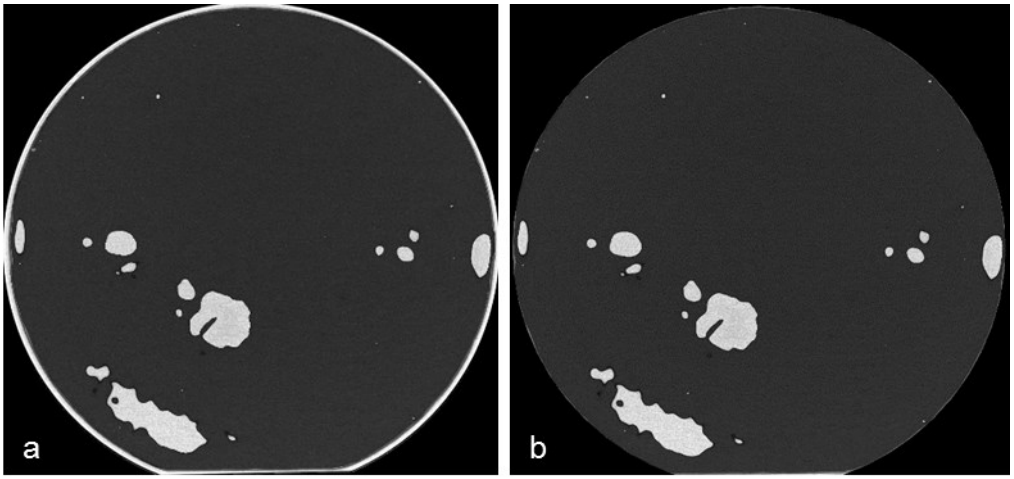

Fig. 15: SAM images of bonded wafers where the bonding layer was fabricated by sputtering. a) Raw image. b) Cropped image.

From the image, bonded areas are indicated as dark-gray (low acoustic reflection) and non-bonded as white (high acoustic reflection). A white ring around the wafer edge can be observed, this non-bonded area is dependent on wafer fabrication method. In order to determine the amount of actual defects in the bonding, the wafer edges have to be excluded. Altered image, where wafer edges have been removed,

is presented above (Fig. 15b). From the cropped image (Fig. 15b) the representative void percentage can be calculated. The edge exclusion and bonded area calculation from SAM images was implemented as Matlab codes presented in Appendixes 1 and 2. The edge exclusion observable in image (Fig. 15a) differed between process methods. It was determined using blank wafers by examination of pixels of the SAM images with MS Paint.

3.8.3 Cross-sectional analysis of the bond interface by Scanning Electron Microscopy

Scanning electron microscopy (SEM) was used in cross-sectional examination of the bond interface. Blanket wafer samples were cleaved using diamond tipped pen from pre-cut wafers. However, in case of patterned wafers this was found to result in poor quality of cross-section. The patterned wafers were diced using Disco DFD651 dicing saw instead. Measurements were performed using LEO SUPRA-35 scanning electron microscope from Leo Electron Microscopy Ltd (currently known as Carl Zeiss) [105]. Images from cleaved and diced wafer were obtained operating the tool using 3.0 kV acceleration voltage with working distance varying form 7 mm to 11 mm. From the images, the presence or lack of bond interface was determined. SEM was also used to measure the structure height of the seal ring after bonding to determine whether the structure had compressed during bonding.

3.8.4 Bond strength determination by maximum shear force

Commonly used razor test was not applicable as it requires IR transparent samples. Shear strength testing was used instead. The tests were carried out using MTS 858 table top system, with adapter tooled for 5 mm x 5 mm chips of standard 150 mm wafers [106]. The tool was found to work even with a smaller chip size of 3 mm x 3 mm. The measurements could be done on samples where SSP silicon wafer was bonded to borosilicate glass wafer. However, bonding two 675 µm thick SSP wafers

resulted in a stack too thick for the measurement setup. A total 12 chips were measured per wafer. The chips were select selected along x and y axis at 3 different radiuses from the wafer center (r_1 = 7 mm, r_2 = 33 mm and r_3 = 57 mm), see Fig. 16.

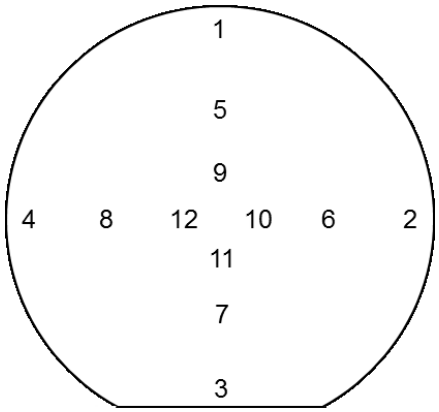

Fig. 16: Sampling of chips for shear strength testing. Twelve chips were tested per wafer; six chips were picked in both vertical and horizontal direction at different distance to wafer edges, for overall coverage of the wafer.

3.8.5 Transmittance

The transmittance was measured using in house build setup that utilized Ocean Optics HL-2000 tungsten halogen lamp as a light source and Ocean Optics Nirquest Near infrared spectrophotometer as a detector. In the measurement set the beam is positioned vertically, detector facing downwards. The wafer was placed in the beam between the light source and detector. Due to support structure of the measurement apparatus wafers were examined at distance of 3-4 cm from wafer edge. Each wafer was measured at 3 points.

3.9 Wafer bonding

The surface oxide is one of the biggest obstacles for good bond quality in low temperatures. The tested oxide removal methods are presented. The bonding parameters and equipment used are presented in detail.

3.9.1 Pre-treatment methods oxide removal before bonding

Three different pretreatment methods were tested, for oxide removal from Cu surfaces. These were formic acid anneal, forming gas anneal and acetic acid wet etch. The formic acid treatment was done *ex situ* in a ATV technologies SRO 704 Solder reflow oven. Due to equipment limitations, only one wafer can be placed in the oven at a time. Which lead to ambient air exposure of the other wafer for duration of over 30 min after the treatment.

Acetic acid pretreatment was performed by dipping the wafers in 10 vol.-% acetic acid solution for 90 s, followed by DI-water rinse and spin-drying. Undiluted glacial acetic acid was also tested. The acetic acid was removed from the wafer surface either with N_2 blow-drying or H_2O rinse followed by spin-drying.

Forming gas anneal was performed *in situ* using the EVG 510 wafer bonder. In fact due to limitations of available equipment the forming gas anneal is the only pretreatment method that could be implemented *in situ*. The anneal was performed using a 10%/90% mixture of H_2 and N_2.

3.9.2 Wafer bonding and post-bonding anneal parameters

The EVG 510 wafer bonder was used for the bonding process. The adjustable process parameters of the tool are: temperature, applied force, time, atmosphere and wafer bow. Since the goal of the bonding was to achieve hermetic encapsulation, the wafers were bonded in vacuum with wafer bow was set “on” for all samples. The bonding tool can pump pressures as low as 10^{-3} mbar in the bonding chamber. Considering the envisioned number of wafers processed with the methods developed in this

work, long bonding time was not considered a hindrance. Therefore, a relatively long bonding time of 60 minutes was used to ensure good bonding. The seal ring widths in cap and MEMS wafers were 80 µm and 60 µm, respectively. The 20 µm difference between MEMS and CAP wafers was used in order to compensate for possible misalignment of wafers.

Overall bonding process is demonstrated in Fig. 17. First the wafers were heated to 200°C, after which the bond chamber was purged twice and a forming gas anneal was applied using 400 mbar for 20 min. After which vacuum was sucked to the bond chamber, the flags separating the wafers were pulled out and temperature increased to bonding temperature (Fig. 17b). At this step the hydraulic piston is brought to contact with top wafer. After reaching the bonding temperature full bonding force is applied for 60 min (Fig. 17c). The bond tool has heating elements in the hydraulic piston and under the bottom wafer. In the first step (Fig. 17a), the heat is only transferred through bottom heater as the piston is not in contact with the top wafer.

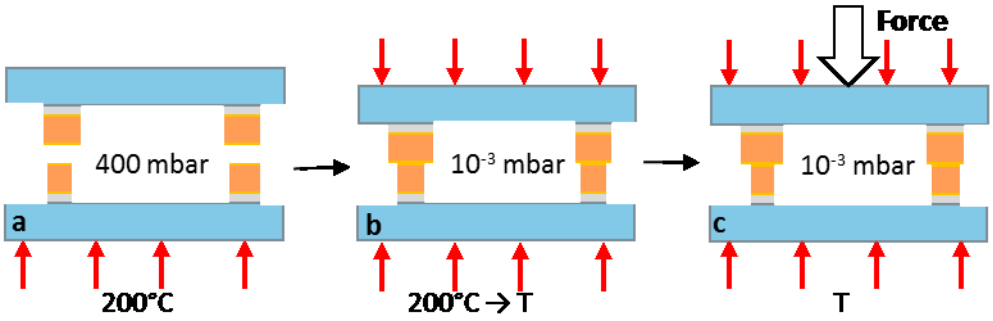

Fig. 17: Depiction of bonding process. a) Wafers are separated by flags and forming gas anneal is applied. b) Vacuum is pumped into bond chamber and flags pulled out. Next, the temperature is increased to bonding temperature T. c) After reaching T, the full bonding force is applied for 60 min.

The two most important process parameters were bonding temperature and applied force. The bonding tool is capable of producing a force of 700-70 000 N, the hydraulic

piston used in the tool cannot produce a stable force on the low end of the range. The effects of the applied force to mitigate adverse effects of surface roughness were studied. Since according to literature high bonding force will lead to better bonding, force minimization was not seen necessary. One of the goals of this work was to develop a bonding method suitable to be used with anti-reflective coated glass wafers tolerating a maximum temperature of 250°C. The exact composition of the coating is proprietary information, which the supplier did not want to reveal. However, AR coatings typically contain several layers of metal oxides such as SiO_2, TiO_2 and MgF, with SiO_2 being the outermost layer [107].

Annealing was done after bonding ones the wafers had cooled down to RT. Cooling took at least two hours. In most of the cases, the annealing was done the day after the bonding. The post-bonding anneal was performed in the bonding tool under N_2 atmosphere at 800 mbar. The wafers were annealed for 60 min without applying any pressure in bonding temperature.

4 Results

The key results of the theses are presented. The focus of the presented results is to demonstrate the effects of temperature and surface topology on bond quality. Effect of used processing methods on the structure of the samples are presented.

4.1 Bonding temperature

The results of non-patterned wafers bonded at different temperatures, while keeping the time and force constant at 60 min and 40 kN, respectively are presented in Table 7. The applied force corresponded to a bonding pressure of 2.6 MPa. The wafer were analyzed by measuring the void area and bond interface. A notably greater percentage of voids can be observed when using the Mark IV. SAM images of the bonded wafers are shown in Fig. 18.

Table 7: Fabrication parameters and bonding results at temperatures between 200°C and 400°C. All wafers were subjected to in situ forming gas anneal for 20 min at 200°C prior to bonding.

Sample	Sputter	surface	Acetic acid	Temperature (°C)	anneal	Voids (%)	Interface
11/12	Mark IV	plated†/plated†	Yes	400	300°C 60 min	2.4	no
13/15	VA	plated†/plated†	Yes	300	300°C 60 min	1.2	no
18/20	VA	plated†/sputtered‡	Yes	250	250°C 60 min	1.7	yes*
21/29	VA	plated†/sputtered‡	Yes	200	-	2.2	no
16/23	VA	plated†/sputtered‡	No	300	300°C 60 min	1.5	-

**Interface was observed on black spotted area. †Bonding layer was fabricated by electroplating 1 µm copper on 300 nm Cu seed layer. ‡Sputtered 1µm bonding layer.*

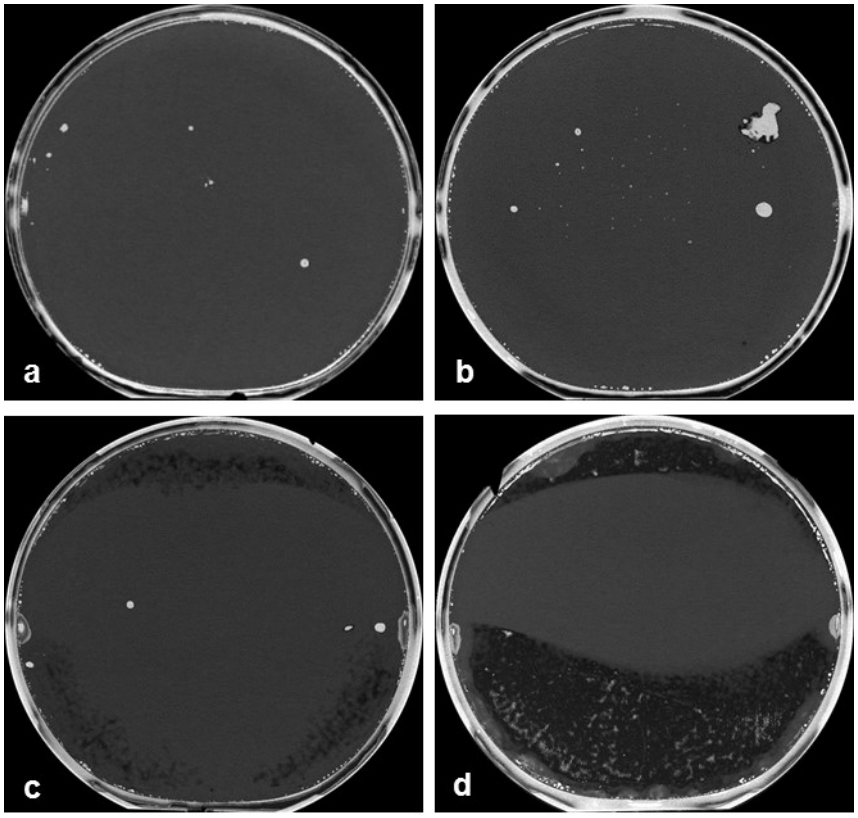

Fig. 18: SAM images of bonded wafers. a) Bonding at 400°C, with 300°C anneal for 60 min. b) Bonding at 300°C, with 300°C anneal for 60 min. c) Bonding at 250°C, with 250°C anneal for 60 min. d) Bonding at 200°C, no post-bonding anneal.

The SAM images show black dotted area around the wafer edge at 250°C (Fig. 18c). At 200°C the black dotted area covers nearly half of the bonding surface (Fig. 18d). The bonded wafers were also examined using SEM. For wafers bonded at 300°C (Fig. 19) and above the original bond interface was not visible. Examining the black spotted region of wafers bonded at 250°C (Fig. 20), the bond interface was found visible.

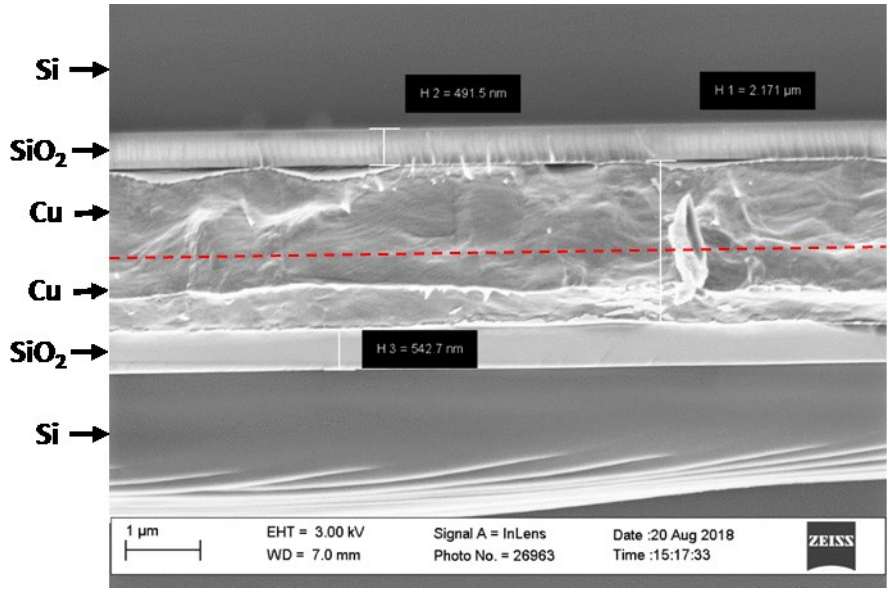

Fig. 19: Cross-sectional SEM image of wafers bonded at 300°C. Original bond interface, marked with red line, is no longer visible.

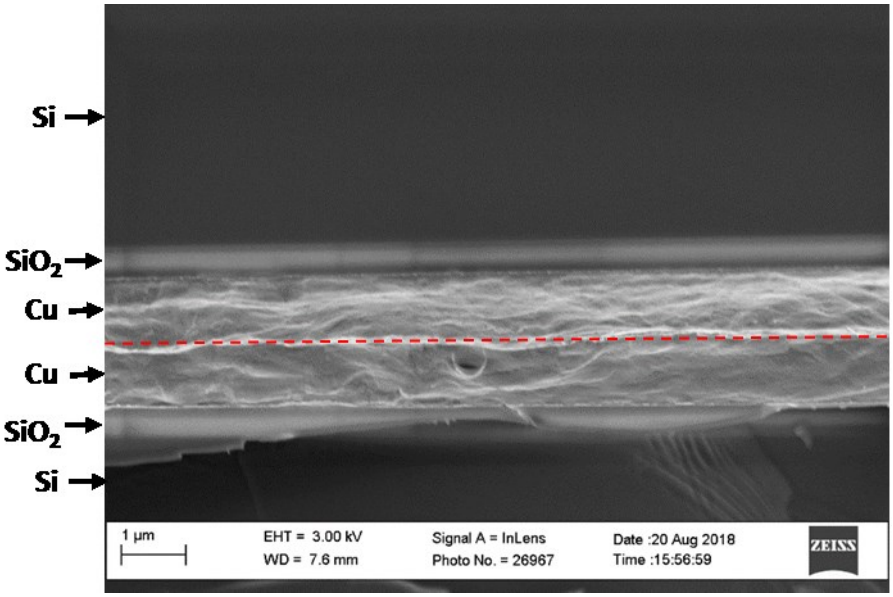

Fig. 20: Cross-section SEM image of black spotted area of wafers bonded at 250°C. Bond interface, marked with red line, is visible between the two copper layers.

4.2 Bonding force

The effect of applied bonding force on the bond quality of patterned wafers (Method 1) to blanket wafers was studied. The wafers were bonded using forces of 3600 N, 5000 N, 7500 N and 20000 N corresponding to bonding pressures of 2.38 MPa, 3.31 MPa, 4.96 MPa and 13.2 MPa respectively. In SAM imaging all of the wafers look similar, there appears to be a void or weakly bonded area in the middle of the seal ring in all wafers. Magnification of a bonded seal ring is presented in Fig. 21b.

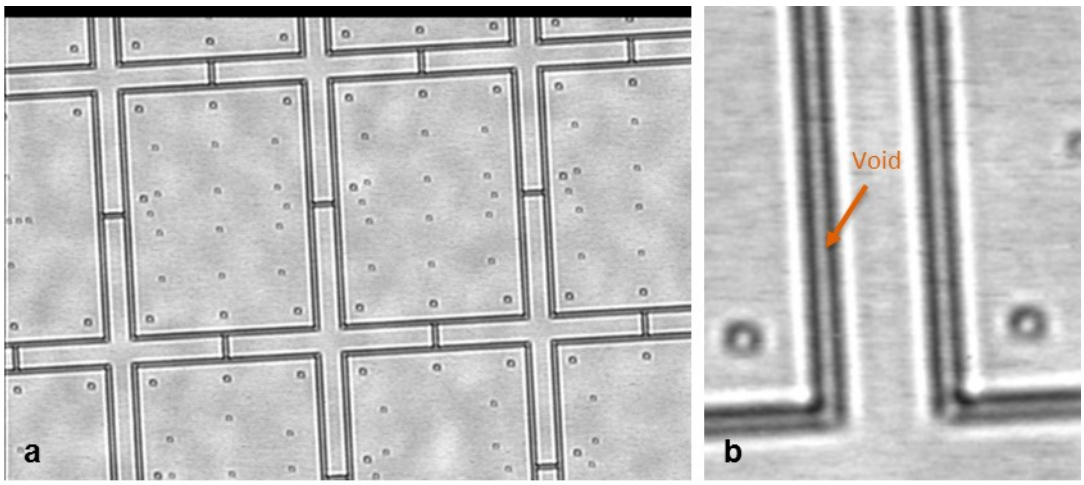

Fig. 21: SAM image of patterned and blank wafer bonded at 300°C. a) The seal rings shown as black and contacts inside the ring shown as dark grey, indicating bonding. b) Magnification, the center of a seal ring (arrow) is shown as light grey, indicating a void or weaker bonding.

The deformation of bond structures during bonding was studied by measuring the structure height of copper seal rings prior to bonding using optical profilometer. After bonding, the cross-section of bonded wafers was examined using SEM. Examining the height of the seal rings before and after bonding revealed a change. Using bonding pressure of 19.8 MPa at 300°C resulted in decrease of 18% in structure height with 60 µm wide seal rings. Annealing similarly bonded sample for 1 h in 300°C resulted in a decrease of 16%.

4.3 Pretreatment

The acetic acid pretreatment was tested using undiluted acetic acid as described in previous study [51]. However, dipping the wafers in 99,8% acetic acid for 90s and drying with N_2 resulted in weak bonding. The samples delaminated during SAM imaging. Using 99,8% acetic acid cleaning followed by H_2O rinse and spin drying did not result in delamination of wafers, they remained firmly together.

Wet pretreatment is not required to obtain good bonding of blanket wafers at bonding temperature of 300°C. SAM image of such wafers is presented in Fig. 22. The Image shows only few voids (1.5%) and uniform bonding across the wafer.

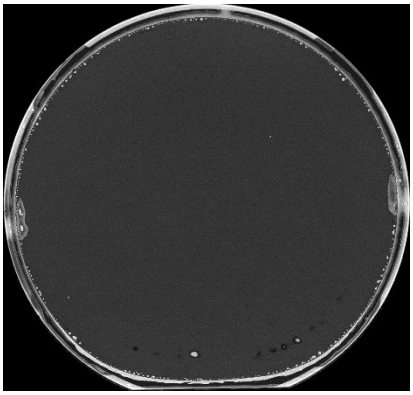

Fig. 22: SAM image of wafers 16/23 bonded at 300°C. No wet pretreatment was used, only pre-bonding anneal in forming gas. The image shows uniform bonding without voids.

4.4 Surface roughness and copper structures

The surface roughness of the seal ring surfaces measured by optical profilometry is presented in Table 8 below. The mean-square-roughness values were determined from measurement data using multiple regional analysis with threshold of 400 nm. A 3D renderings of the samples of Table 8 are shown below in Fig. 23. Clear differences

in the surface quality can be observed, in accordance with data of Table 8. The surface roughness of the Cu film after sputtering on von Ardenne was 6.6 nm.

Table 8: Surface roughness of Cu structures fabricated by different methods.

Sample ID	Copper film	Etchant	Bonding layer exposed	Structure height (nm)	Rq (nm)
w46	plated	H_3PO_4	Yes	2189	148
w48	plated	$Na_2S_2O_8$	yes	1545	200
w49	sputtered	H_3PO_4	no	1862	80
w50	sputtered	$Na_2S_2O_8$	no	1867	34

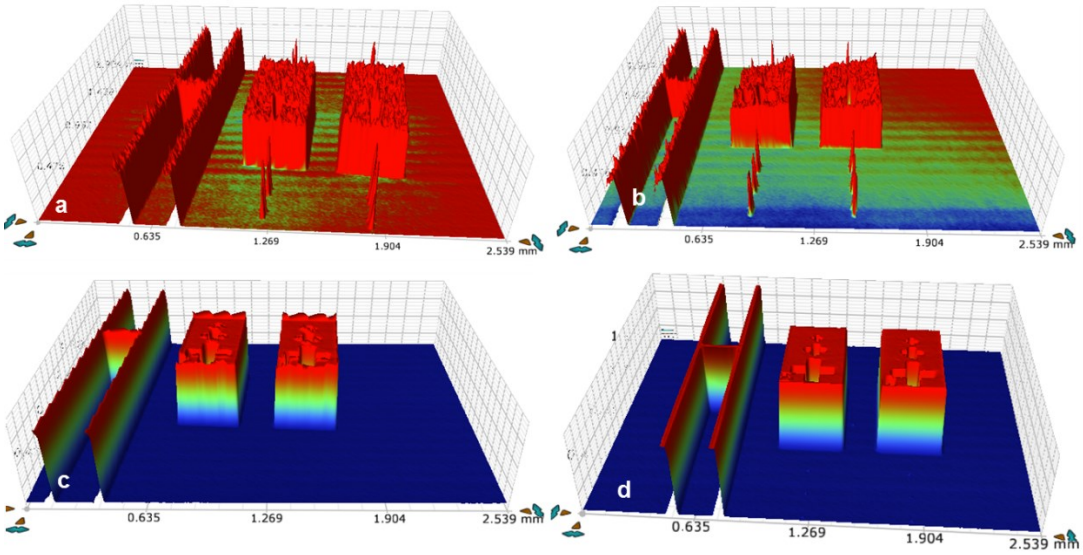

Fig. 23: 3D images of optical profilometry data. a-b): Pattern produced via electro-plating with resist mask and etching the seed layer (Method 2) using either: a) H_3PO_4 based or b) $Na_2S_2O_8$ based etchant. c-d): Pattern produced by etching from sputtered film (Method 3) using: c) H_3PO_4 or d) $Na_2S_2O_8$.

The 3D renderings show that exposing the bonding surface to etchants (Method 2) will result in high surface roughness regardless of etchant. Covering the bond surface

(Method 3) during exposure to etchant will result in smoother surfaces. Of the etchants $Na_2S_2O_8$ (Fig. 23d) was better as it did not produce rough edge structures like H_3PO_4 based solution (Fig. 23c).

Microscopy examination reveals a clear difference in fabricated structures between the microfabrication methods (Fig. 24). Methods 1 and 3, where the structure is created by etching, are result in under etching. In Fig. 24a the photoresist patterns of the electric contacts (light gray) and the actual etched copper structures (yellowish orange) are visible. It can be seen that the copper patterns have significantly receded under the resist. The etchant has corroded copper under the resist so that in some cases the contacts had been etched completely. While under etching destroys the contacts (width = 20 µm), the wider seal rings (width = 60 nm) have remained continuous (Fig. 24b). However, method 2 can produce desired shape contacts. As the exposure in that method to etchant is shorter, the smaller structures remain undamaged/sufficiently wide. Image of bonded contacts produced by Method 2 is presented in Fig. 24c.

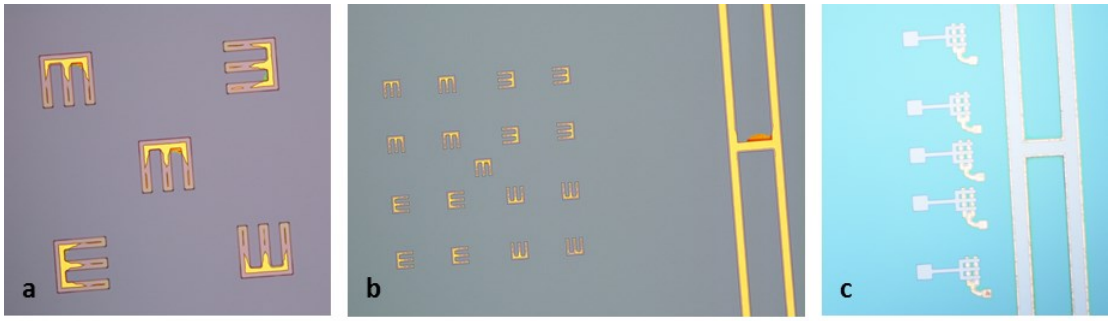

Fig. 24: a and b) Microscope image of Cu structure fabricated by the Method 1 shows strong under etching on E-shaped contacts inside the bond frame. As a result the contacts could not be bonded. c) Microscope image of bonded wafers fabricated by the Method 2 shows no under etching on the bonded contacts.

The differences in bonding between etched and electroplated structures are further demonstrated by SAM image (Fig. 25) of bonded wafers. Sample in Fig. 25a is fabricated by Method 3 and as suspected from microscope images the seal ring has bonded (visible as gray lines) but the contacts have not (not visible at all). On the contrary, using Method 2 results in bonding of both seal rings and contacts inside them, as seen in Fig. 25b.

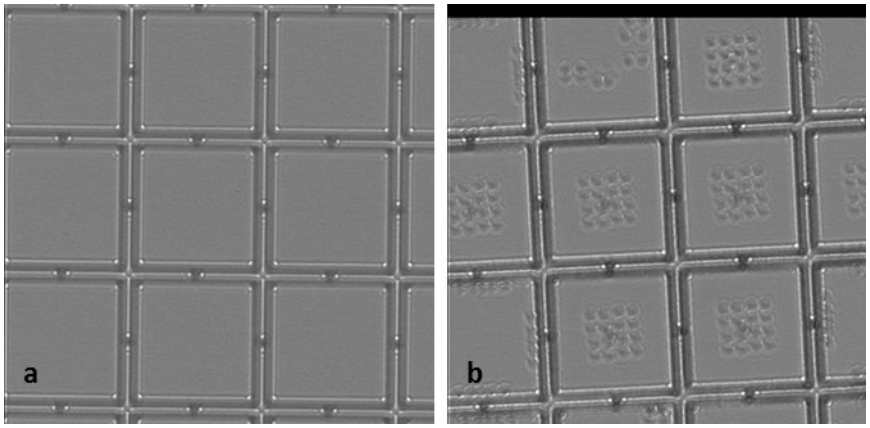

Fig. 25: SAM image of bonded wafers. a) Wafers fabricated by the Method 3 show seal rings as black lines indicating bonding but the E-shaped contacts cannot be seen at all indicating no bonding at all. b) Wafers fabricated by the Method 2 show both seal rings and contacts as black or dark gray lines indicating bonding.

Besides etchant, also the choice of resist stripping equipment had an influence on the copper pattern profiles. Two tools were used in resist stripping prior to electroplating: the PRS 900 and the RIE Oxford 80plus. In Fig. 26 the height profiles of the copper structures after electroplating and resist removal are shown. In Fig. 26a the resist was stripped using PRS 900, whereas in Fig. 26b the resist was stripped using RIE Oxford 80plus. The use of the PRS 900 results in a distinct “bull horn” shape where the height difference between seal ring edges and center is around 200 nm. With RIE Oxford 80plus resist stripping the seal ring surface is more even, the height difference being only around 50 nm.

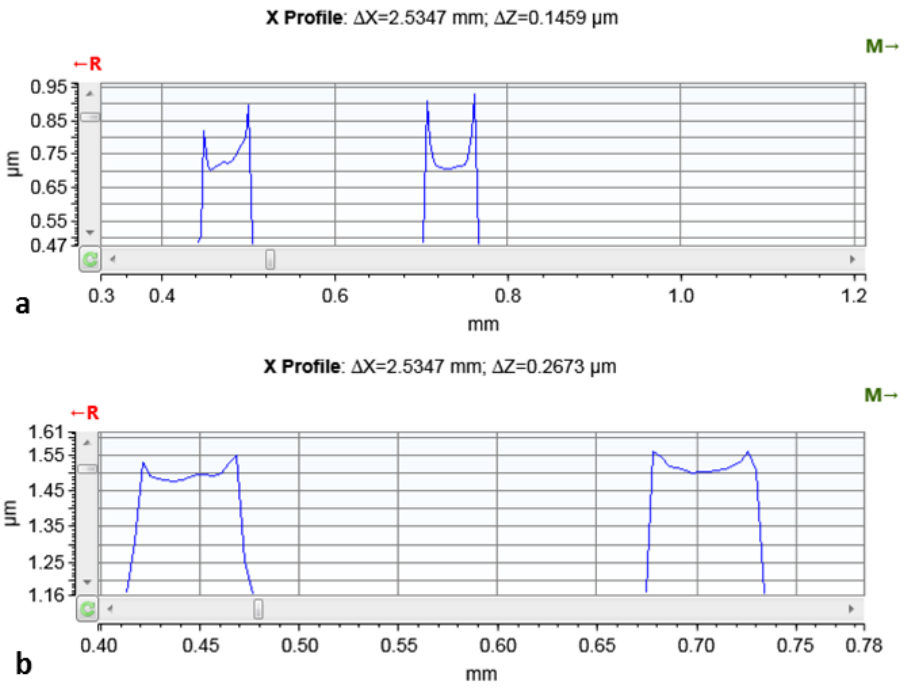

Fig. 26: Optical profilometry side profile of plated copper seal rings. a) Resist stripping using Oxford PRS 900 resulted in large height difference between the edge and the center of the seal ring. b) Resist stripping using RIE Oxford 80plus, less height difference between the center and edges of plated copper structure.

4.5 Bond strength and dicing

Glass wafers were bonded to silicon wafers at 250°C as the anti-reflective coating poses such thermal limitations. Various pretreatment methods and two different microfabrication methods were tested. The tested methods were Method2 (electrodeposition through a resist mask) and method 3 (etching from sputtered copper using image reversal resist). All wafer were subjected in situ forming gas anneal prior to bonding and bonded for duration of 60 min. During bonding, the wafers were subjected to a force of 30 kN resulting in a bonding pressure of 19.8 MPa. Experiments are listed in detail in Table 9.

Table 9: Tests done using silicon MEMS and glass cap wafers. The shear strength column indicates the strength of the bond measured as maximum shear strength, measured using shear stress test.

Sample	Fabrication method	pre-treatment method	Bonding Temp. (°C)	Anneal	Shear strength (MPa)	notes
42/G7	Method 2	10% Acetic acid, H_2O rinse, spin dry	300	no	77 ± 34	
44/G11	Method 2	10% Acetic acid, H_2O rinse, spin dry	250	no		
45/G8	Method 2	10% Acetic acid, H_2O rinse, spin dry	200	no	55 ± 20	
46/G9	Method 2	99.8% Acetic acid, N_2 blow dry	250	no	-	Delamination during SAM.
47/G12	Method 2	99.8% Acetic acid, H_2O rinse, spin dry	250	no	46 ± 17	
48/G14	Method 2	99.8% Acetic acid, H_2O rinse, spin dry	250	no	44 ± 12	Etched with $Na_2S_2O_8$
49/G16	Method 3	99.8% Acetic acid, H_2O rinse, spin dry	250	no	113 ± 21	Small under etching (H_3PO_4), strong under cut in resist
50/G17	Method 3	99.8% Acetic acid, H_2O rinse, spin dry	250	no	150 ± 20	Smoothest surface, $Na_2S_2O_8$ etching
51/G26	Method 3	99.8% Acetic acid, H_2O rinse, spin dry	250	yes†	40 ± 16	AR coat, strong under etching in contacts ($Na_2S_2O_8$)
52/G28	Method 3	99.8% Acetic acid, H_2O rinse, spin dry	200	yes†	75 ± 22	AR coat, strong under etching in contacts ($Na_2S_2O_8$)

† Annealing was performed in 800 mbar N_2 for 60 min at the bonding temperature, the anneal was performed in the bond tool.

On visual inspection after dicing, delamination was observed on all wafers fabricated using Method 2. For the samples fabricated using method 3 no such delamination was observed. This finding suggests higher interfacial adhesion on samples fabricated via Method 3 as compared to samples fabricated via Method 2. For example, at 250°C bonding temperature shear strengths of 46 MPa and 150 MPa could be achieved for methods 2 and 3, respectively. The cause of failure for samples fabricated by Method 2 was primarily sliding as the two bond frames separated along the bond interface. However, over half of the chips fabricated with Method 3 failed due to fracture of substrate indicating a stronger bond than the substrates. No clear correlation was found between bond strength and chip's distance from the center of the wafer.

The delamination resulting from the dicing is presented in photograph (Fig. 27). The amount of delamination is dependent on sample fabrication method, being larger for Method 2. The delamination starts from the edges propagating towards center of the wafer. In dicing, different saw blades had to be used for the glass and silicon wafer and the delamination of the top wafer damaged the dicing blade.

Three wafers (51/G26, 52/G28 and 47/G12) fabricated by Methods 2 and 3 were diced fully into chips. From these wafers, the dicing yield was calculated as number of chips not delaminated divided by the total number of chips on wafer. The results are presented in Table 10. Bonding AR-coated glass cap wafer into silicon wafer at the temperature of 250°C resulted in superb dicing yield of 99%, while bonding at 200°C a yield of 97% was obtained. For wafers fabricated by Method 2 there seems to be more variation between wafers, however a dicing yield of 94% was reached with wafers bonded at 250°C.

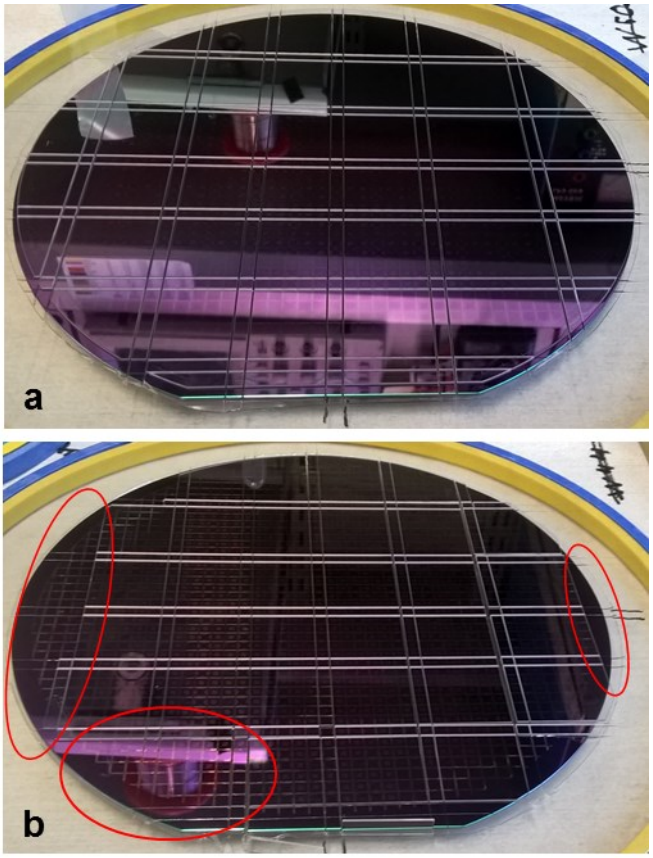

Fig. 27: Images of diced wafers. a) In wafer 49/G16 fabricated by Method 3, no de-lamination is observed. b) In wafer 48/G14 fabricated by Method 2, part of the wafer had delaminated during dicing. The delaminated areas are indicated with red ellipses.

Table 10: Dicing yield of wafers fabricated via Methods 2 and 3.

Sample	Fabrication method	Delaminated chips	total chips	Yield
51/G26	Method 3	18	1433	99 %
52/G28	Method 3	38	1433	97 %
47/G12	Method 2	87	1433	94%

4.6 Optical transmittance of anti-reflective film.

The optical transmittance was measured from borosilicate glass wafers and antireflective coated borosilicate glass wafers. The effect of temperature on performance of AR-coating is reported in Fig. 28. For the application in which the packaged MEMS mirrors are to be used most significant is the transmittance at the wavelength of 950 nm. The results presented are an arithmetic mean of three measurement points on same wafer and they are presented in Table 11. AR-coated wafers have 6.1 % improvement in transmittance. Lower transmittance and higher deviation is measured in wafer obtaining patterned metal film. No difference is observed between light passing through front or backside of the wafer.

Table 11: The effect of Anti-reflective coating, thermal treatment and bond structures on optical transmittance at 950 nm.

Sample	AR coating	Thermal treatment	Bonding structures	Transmittance
1	No	No	No	93.5 ± 0.71 %
2	Yes	No	No	99.2 ± 0.30 %
3	Yes	200°C	No	99.9 ± 0.45 %
4	Yes	250°C	No	100.8 ± 0.21 %
5	Yes	No	Yes, Front side	92.5 ± 2.35 %
6	Yes	No	Yes, Backside	92.5 ± 2.95 %

The wafers with patterned metal film (sample 5 and 6) are plotted against borosilicate glass (sample 1) and untreated AR-coated glass (sample 2) wafers in Fig. 29. In the middle of the spectrum sample 2 is observed to have highest transmittance. However, near the ends of the measured spectrum glass (sample 1) has the best transmittance. The spectrum of samples 5 and 6 has the same shape as with sample 2 however the transmittance is lower.

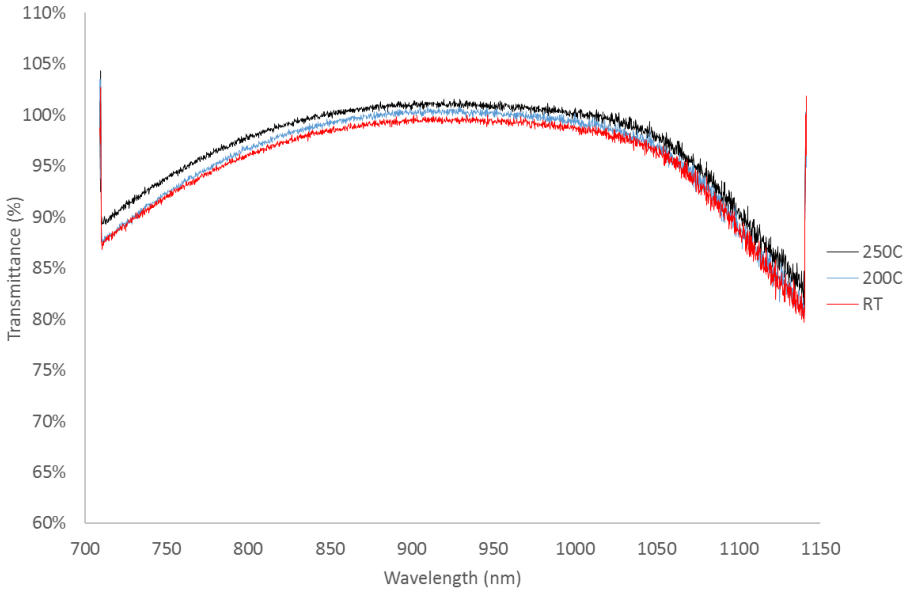

Fig. 28: Transmittance as a function of wavelength. Measured on AR-coated borosilicate wafers. Black) Thermal treatment at 250°C. Blue) Thermal treatment at 200°C. Red) No thermal treatment.

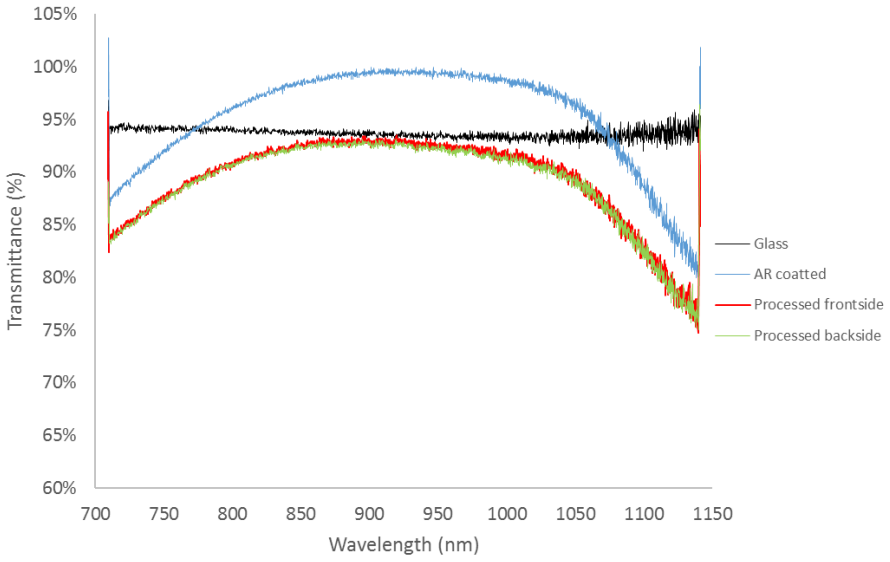

Fig. 29: Transmittance as a function of time. Black) Borosilicate glass with no processing. Blue) AR coated borosilicate glass before processing. Red) AR coated borosilicate glass wafer with fabricated bonding structure. Beam enters from the front side. Green) AR coated borosilicate glass wafer with fabricated bonding structure. Beam enters from the backside.

5 Discussion

The key results are discussed in this chapter. Influence of measurement setup on obtained results is explained and the obtained results are compared to previous studies. The topics of greatest interest are the bonding temperature and pretreatment as well as the surface topology of bond structures.

5.1 Temperature and pretreatment

SAM images reveal good bonding across the wafer at 400°C and 300°C. There are very small number of voids, and the original bond interface was no longer visible in SEM cross-section. The absence of distinct bond interface indicates good diffusion between Cu, there is no longer two individual Cu films as they have merged into one. This indicates a good bond quality.

Lowering the temperature to 250°C or 200°C reduced the bond quality. SAM image (Fig. 18) reveals black spotted area on wafer. SEM cross-section images confirmed that the black spots are a result of a distinct bond interface. SAM image of wafers bonded at lowest temperature of 200°C has white spots mixed with the black indicating voids to be present in the area.

The bond interface indicates that there has not been sufficient grain growth between the bonding films. Based on the observations lowering the bonding temperature below 300°C will be problematic for maintaining good bond quality. Therefore, further measures need to be taken to improve the bond quality at these low temperatures.

Increasing the applied bonding pressure was not possible using whole wafers since the bonding tool can produce a maximum force of 70 kN. Patterned wafers were used in the remaining tests, increasing the local bonding pressure. On patterned wafers, the bonding pressure, being equal to force divided by the pattern area, is orders of magnitude higher due to the correspondingly lower surface area. Due to the increased pressure, patterned wafers could be successfully bonded at temperatures as

low as 200°C, well below the thermal limit set by the antireflective coating. The mechanical strength did not differ significantly between bonding in 200°C or 250°C, when the structure was fabricated using Method 2. However, notable increase of 40 % in the bond strength was observed, when bonding temperature was increased from 200°C to 300°C.

The results are in line with previous studies. Fan *et al.* have successfully thermocompression bonded copper in temperatures as low as 250°C [75]. The formed bond was hermetic. The method used by Fan *et al.* included *ex situ* acetic acid wet etch but no further *in situ* treatments [75]. Rebhan *et al.* have bonded copper at 200°C with sufficient bonding quality [43]. Their method comprised of *ex situ* citric acid and *in situ* forming gas treatment. Thermocompression bonding copper has been recorded as low as in room temperature using proprietary surface activation [19]. However, in that case the bonding did require further annealing in 200°C.

Based on literature, the acetic acid pretreatment method was changed from dilute 10% acetic acid to glacial acetic acid [51]. As formation of copper(II) hydroxide in presence of water was a concern, blow-drying the wafer after acid dip was attempted. However, using glacial acetic acid pretreatment followed by N_2 blow drying resulted in delamination of wafers after bonding. Results are contradictory to previous studies [40], [54], [75]. Fan *et al.* had used *ex situ* acetic acid pretreatment with N_2 blow-drying with good results [75]. When the glacial acetic acid treatment was followed by H_2O rinse and spin-drying no delamination occurred. This suggests that the N_2 gas drying could not remove the acetic acid fully from the bond surface, perhaps due to the microstructure on the wafers. Leaving layer interfering with the bonding on the wafer. In this situation having H_2O rinse and spin dry proved to provide better bonding results. Spin-drying without H_2O rinse was not attempted as contamination of spin rinse dryer should be avoided.

When increased bonding temperature is used *ex situ* treatment is unnecessary. Good bonding of blank wafers at 300°C was observed with using only *in situ* forming gas

pre-treatment. Voids covered only 1.5% of the bond area (Fig. 22), which is comparable to samples with wet pretreatment.

5.2 Surface roughness and microfabrication

The built-in surface roughness software of the optical profilometer contour seems to give remarkably different values for root-mean-square-roughness depending on measurement settings rather than sample topography. The main problem seemed to be in built-in software's capability to recognize the structures from background. As such, the obtained numerical values can be considered more as trends than exact values. Therefore, conclusions have to be drawn based on observations from the 3D images. Judging from the image (Fig. 23) the Fig. 23d has smoothest surface, formed using Method 3 where the copper is etched using sodium persulfate. When phosphate acid based etchant is used (Fig. 23c) there seems to remain a rough edge around the areas covered by resist. Regardless of etchant, using Method 2 produces a rough surface (Fig. 23a and Fig. 23b) since the pattern is exposed to the etchant.

Two sputtering systems were used in the thesis MRC TEL Eclipse Mark IV and Von Ardenne CS730 S. The TEL Eclipse Mark IV was used on only one pair of wafers as, inspecting the wafers with optical profilometer revealed particle contamination. No contamination was found on wafer sputtered using von Ardenne and hence it was used for all other samples in the thesis. The previously reported surface roughness is in line with measured, the Von Ardenne CS730 S sputtering system had R_q of 6.6 nm before patterning. Surface roughness (R_q) of 15 nm has been recorded for DC sputtered copper of 1000 nm film thickness [108]. Whereas, Rebham et al. have measured sputtered copper at Rq = 8 nm [57]. Using chemical mechanical polishing (CMP) the roughness can be reduced to 2 nm [57].

As there were no previously developed process for fabrication of copper seal rings at VTT, the methods developed in this work required significant optimization. Especially Method 3, where the significant resist undercut in the image reversal step needed to be addressed. The size of the undercut is dependent on three parameters: exposure

time, reversal bake temperature, time and resist development duration. As eliminating the undercut of the image reversal resist AZ5214 proved to be unexpectedly difficult, new masks with opposite polarity were obtained. Hence, the fabrication Method 1 could be utilized.

Of the two tools used for the resist stripping RIE Oxford 80plus is clearly a better choice by producing more uniform surface on electrodeposited structures. The impact of the stripping tool on the electroplated structures is likely caused by the operating temperature of the tool. While RIE Oxford 80plus operates at RT thanks to water cooling, the Oxford PRS 900 is used at elevated temperatures near 120°C. The high temperature will cause the thick AZ9260 photoresist to deform, resulting in change in resist wall geometry.

As previously described, using $Na_2S_2O_8$ solution for etching produced better surface structure in Method 3. However, when using Method 2 there is no notable difference in surface roughness between H_3PO_4 based and $Na_2S_2O_8$ based etchants. The bond strength difference between samples etched with the two etchants was well within the measurement uncertainty. With Method 3, using $Na_2S_2O_8$ results in a 33% increase in shear strength, which is from 113±21 MPa to 150±20 MPa. This increase is clearly outside the standard deviation of the sample.

Light gray area, indicating a weak bonding or a void, is visible inside a seal ring in SAM image (Fig. 21) of bonded wafers fabricated using Method 1. The Light grey area may also be result of insufficient resolution of the SAM. Cross-sectional SEM imaging was attempted to confirm the matter. However, the fabricated structure lead to uneven cleaving of the sample and dicing the wafers using dicing saw resulted in rough cross-section surface, hence no clear images could be taken from the seal ring structure.

Measuring the seal ring structure height before and after bonding revealed a height loss of 16%-18%. The results are surprising as Cu is known to have very little deformation during the bond process as it remains in solid form during the whole process. The difference can be explained by the different methods used for measuring the structure height before and after bonding. Namely, before bonding the structure

height was measured using optical profilometer. The transparent SiO_2 layer had interfered with the measurement, resulting in the profilometers inability to measure the background correctly.

5.3 Mechanical testing

Samples for shear force measurement were picked from all over the wafer as demonstrated in Fig. 16. From the measurement, it can be clearly seen that there is rather large variation between samples. As dicing resulted in delamination around the edge of some of the wafers, this meant that chips close to wafer edge could not be used in shear testing. From chips surviving the dicing, no clear correlation between chip's distance from center of the wafer and bond strength could be observed. This is rather unexpected, as from the higher delamination rate one would think the near-to-edge chips would have a lower bond strength. Therefore, one can draw a conclusion that the edge chips with low bond strength must have delaminated during dicing. The shear strength values presented in Table 9 are the average of multiple chips measured from the same wafer, and as lower adhesion "edge" chips could not be measured, is the average subjected to survivorship bias.

Due to substrate material strength, the measurement setup could not fully measure the high end of bond strength. In the shear force measurement of wafers fabricated using the Method 3, many of the samples shattered the silicon and glass substrates breaking into pieces. This suggests that the adhesion between the two copper interfaces is higher than what could be measured. A reason for the substrate breaking could be in uneven distribution of load during measurement, as the tool is designed for larger (5 mm x 5 mm) chip size. In addition, in fabrication Method 3 under etching of seal rings was observed, thus the seal ring width is narrower than intended in the mask design. As a result, the real bonding area is smaller than calculated from a mask file and hence the true shear strength is higher than reported. Example of a measurement is provided in Appendix 4.

Because of multiple bond strength measurement methods used in literature, making a direct comparison is problematic. Bond strength of 130 MPa has been reported for acetic acid cleaned sputtered Cu bonded at 400°C for 1h [109]. For ECD flycut Cu bond strength of as high as 208 MPa has been reported when citric acid pre-treatment was used and the wafers were bonded at 250°C [110]. The shear test results are in same order as aluminum thermocompression bonding. Aluminum has shear strength of 52.2 ± 37.8 MPa at 360°C [90]. The correlation between bonding temperature and bond strength is in line with previous studies. Chen *et al.* have reported tensile strengths of 32 MPa, 27 MPa and 14 MPa for wafers bonded in 300°C, 250°C and 200°C, respectively [88].

5.4 Optical transmittance

The optical transmittance of the wafers was within the expected range. Plan Optik claims the wafers to have reflectance of less than 0.5% at 905 nm on each side [111]. Based on the measured transmittance the untreated and thermally treated samples in line with the distributor's statement. However, the processed wafer containing Cu seal rings is not. The optical transmittance of the wafer is even lower than a glass wafers. The lower transmittance is most likely result of the metal film interfering with the light. The light beam used to measure the transmittance was so wide that the seal rings blocked part of the beam from hitting the detector. In addition, the shape of the transmittance spectrum is similar to AR-coated sample that was not exposed to heat or process environment. If the AR-coating had been damaged in the process the shape of the spectrum would be different as the sample composition is no longer the same.

6 Conclusions

The surface roughness was found to be the most significant factor in obtaining good bond quality. Exposing the bonding surface to etchant was found to increase the surface roughness and lead to weaker bonding.

Covering the bonding surface with photoresist during etching increased the bond strength and dicing yield. While etching the structure form 1 µm Cu film did improve the bonding, it was also problematic. Prolonged exposure to etchant caused under etching which was detrimental to small structures. The 20 µm wide electric contacts were nearly completely etched, and could not be bonded. On the other hand, in electrodeposited samples, where the only Cu seed layer need to be etched, the exposure to etchant was shorter. Due to shorter exposure the 20 µm wide structures were only slightly etch and could be bonded. If the electric contacts to device are made through silicon via in cap wafer, the under etching of smaller structures will cause problems.

The best bonding quality was obtained, when the samples were fabricated from sputtered 1 µm Cu film by etching with sodium persulfate and *ex situ* acetic acid treatment and *in situ* forming gas anneal were used. Even at as low temperature as 200°C a superb dicing yield of 97% was achieved. The bond strength was recorded at 75 MPa, over ten times the MIL-STD-883E standard defined rejection limit of 6.08 MPa. Good results at 200°C suggest that, the copper thermocompression bonding could be possible in even lower temperatures. Bonding in lower temperatures was not attempted in this study. Further studies need to be made to determine the lowest possible temperature for thermocompression bonding.

The anti-reflective coating was confirmed to remain unchanged by thermal treatment at 250°C and exposure to process environment used in bond structure fabrication. The transmittance was measured at 99.9 % at wavelength of 950 nm after heat treatment in 250°C. The AR-coating provides a significant improvement in transmittance compared to borosilicate glass without a coating (93.5 %).

For some applications, the problem of under etching in seal ring fabrication could be avoided by fabricating the rings via lift-off method. Further studies needs to be made on the viability of lift-off, the method was not attempted in the thesis due to concerns of substrate heating during sputtering. The results show that patterned structures can be bonded in lower temperatures than blank wafers. This is likely due to higher bonding pressure of patterned wafers, resulting from smaller bond area.

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A Appendix 1: Matlab code for graphics data processing of SAM images

The programming code is presented below and based on previous code by Galarnyk [112].

```
%code by Michael James Kali Galarnyk at stack overfolw:
%https://stackoverflow.com/questions/11079781/cropping-an-ellipse-from-an-image,
%read 19.10.2018

%citation begins
[FileName,PathName] = uigetfile({'*.jpg;*.tif;*.png;*.gif','All Image Files'},'Please Select an Image');
image = imread([PathName FileName]);
imshow(image) %needed to use imellipse
user_defined_ellipse = imellipse(gca, []); % creates user defined ellipse object.
wait(user_defined_ellipse); % You need to click twice to continue.
MASK = double(user_defined_ellipse.createMask());
new_image_name = [PathName 'Cropped_Image_2_' FileName];
new_image_name = new_image_name(1:strfind(new_image_name,'.')-1); %removing the .jpg, .tiff, etc
new_image_name = [new_image_name '.png']; % making the image .png so it can be transparent
imwrite(image, new_image_name,'png','Alpha',MASK);

%citation ends

%cropping the flat
image = imread(new_image_name,'png');
J = imcrop(image);
figure, imshow(J);
imwrite(J, new_image_name,'png');
%End of program
```

B Appendix 2: Matlab code for determination of bonding percentage

The programming code is presented below and loosely based on an uncredited example in MathWorks web pages [113].

```
%Start of program
file_name = uigetfile('*.*');              %Input from user
image = imread(file_name);                 %read file to variable
figure, imshow(image), title('SAM image')  %shows raw SAM-image

nro_colors = 3;       %no. of clusters
% repeat the clustering 3 times to avoid local minima?
pixel_labels = imsegkmeans(image,nro_colors,'NumAttempts',3);

figure, imshow(pixel_labels,[])
title('Image Labeled by Cluster Index');

% lables each cluster as a mask
mask1 = pixel_labels==1;
cluster1 = image .* uint8(mask1);
figure, imshow(cluster1)
title('Objects in Cluster 1');

mask2 = pixel_labels==2;
cluster2 = image .* uint8(mask2);
figure, imshow(cluster2)
title('Objects in Cluster 2');

mask3 = pixel_labels==3;
cluster3 = image .* uint8(mask3);
figure, imshow(cluster3)
title('Objects in Cluster 3');

% Calculating the pixels in each cluster

cluster1_totpx = numel(cluster1);   %total number of pixels in the cluster
cluster1_NB = length( cluster1(cluster1~=0) );  %nro. of pixels not black in cluster

cluster2_totpx = numel(cluster2);   %total number of pixels in the cluster
cluster2_NB = length( cluster2(cluster2~=0) );  %nro. of pixels not black in cluster
```

```
cluster3_totpx = numel(cluster3);   %total number of pixels in the cluster
cluster3_NB = length( cluster3(cluster3~=0) );  %nro. of pixels not black in cluster
%%
bond_area = 0;   %Setting the bond area value to 0
void_area = 0;   %Setting void area value to 0
other_area = 0;
pixel_list = [cluster1_NB, cluster2_NB, cluster3_NB];  %list !!!!????
%user input loop
for i = 1:3
   promt = sprintf('Is cluster %i bonded: (1=bonded; 2=void; 3=other) \n', i);
   cluster_inp = input(promt, 's');
   if cluster_inp == '1'
      bond_area = bond_area + pixel_list(i);
   elseif cluster_inp == '2'
      void_area = void_area + pixel_list(i);
   elseif cluster_inp == '3'
      other_area = other_area + pixel_list(i);
   else
      fprintf('Invalid user input \n');
   end
end
%void precentage
wafer_area = bond_area + void_area + other_area;  %total number of pixel in a single
wafer
bond_percent = (bond_area/wafer_area)*100; % Calculating the persentage of
bonded area.
void_percent = (void_area/wafer_area)*100; % Calculating the persentage of void
area.
other_percent = (other_area/wafer_area)*100;
%prints the calculated results
fprintf('From the total wafer area %.2f %% has bonded.\n', bond_percent);
fprintf('Voids: %.2f %% \n', void_percent);
fprintf('Other: %.2f %% \n', other_percent);
%End of program
```

C Appendix 3: Microfabrication parameters

Key fabrication parameters are presented in this appendix. The electrodeposition of copper was carried out using RENA EPM 201 F by RENA Technologies. The parameters used are listed below in table (Table 12).

Table 12: Electrodeposition parameters.

	Method 1	Method 2
Resist mask	no	yes
Plating time (min)	5	15
Plating area (cm^2)	154	10.6-14.1
Set current (mA)	1540	120-150
Recorded voltage (V)	1.3-1.5	0.3-0.7
electrolyte flow (l/min)	20	20
rotation (RPM)	10	10
Plating temperature (°C)	24-25	24-25

The resist coating step was done using resist station Gamma from SUSS MicroTec. Below (Table 13) are listed the key process parameters of the resist coating, note that spinning speed and time are not listed as the spinner operates in solvent atmosphere and is therefore not comparable to spinning speeds reported in literature.

Table 13: Key process parameters corresponding to recipes used in the thesis.

Recipe	Vapor-prime (HDMS)	Cool plate	Spincoat	Resist	Edge bead re-moval	Hot plate	Cool plate
Q-C-NIC-6in-R3-7µm-Pr-EBR	30s	22°C 60s	7.1 µm	AZ9260	yes	110°C 300s	22°C 60s
Q-C-NIC-6in-R3-7µm-Pr-NEBR	30s	22°C 60s	7.1 µm	AZ9260	no	110°C 300s	22°C 60s
Q-C-NIC-6in-R2-1.5µm-Pr-NEBR	30s	22°C 10s	1.5 µm	AZ5214E	no	90°C 60s	22°C 10s

D Appendix 4: Shear force measurement

Below (Table 14) is an exemplary shear force measurement, in sample column the number indicates the location of the chip on wafer in reference to Fig. 16. Slide or break column tells the failure mechanism of the sample, whether the two slide across one another or whether the substrate broke. Shear force is the highest measured force the sample could withstand before breaking.

Samples B2 and B3 had delaminated during dicing and were excluded when calculating the average, sample B9 had exceptionally low shear force and was excluded as an outlier.

Table 14: Shear force measurement of a wafer bonded using Method 2. Samples B2 and B3 had delaminated during dicing, high variance between the chips.

Wafer ID	Description	sample	Slide or break	Shear force (N)	Avr. Force (N)	Std. Force (N)	Avr. Shear strength (MPa)	Std. Shear strength (MPa)
w42/G7	Delaminated around the wafer edge.	B1	slide	24.7	54.34	24.16	77.01	34.26
		B2		-				
		B3		-				
		B4	slide	57.47				
		B5	slide	30.22				
		B6	break	85.59				
		B7	break	85.11				
		B8	slide	53.35				
		B9	slide	13.47				
		B10	slide	43.91				